Actel Extended Temperature Fusion Family of Mixed Signal FPGAs

FlashLock

Features and Benefits

Extended Temperature Tested

- Each Device Tested from –55°C to 100°C Junction Temperature

High-Performance Reprogrammable Flash Technology

- Advanced 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Nonvolatile, Retains Program when Powered Off
- Live at Power-Up (LAPU) Single-Chip Solution
- 350 MHz System Performance

Embedded Flash Memory

- User Flash Memory – 4 Mbits to 8 Mbits
  - Configurable 16- or 32-Bit Datapath
  - 10 ns Access in Read-Ahead Mode
- 1 Kbit of Additional FlashROM

Integrated A/D Converter (ADC) and Analog I/O

- Up to 12-Bit Resolution and Up to 600 Ksps
- Internal 2.56 V or External Reference Voltage
- ADC: 30 Scalable Analog Input Channels
- High-Voltage Input Tolerance: –10.5 V to +12 V
- Current Monitor† and Temperature Monitor Blocks
- Up to 10 MOSFET Gate Driver Outputs
  - P- and N-Channel Power MOSFET Support
  - Programmable 1, 3, 10, 30 µA, and 20 mA Drive Strengths
- ADC Accuracy Is Better than 1%

On-Chip Clocking Support

- Internal 100 MHz RC Oscillator (Accurate to 1%)
- Crystal Oscillator Support (32 KHz to 20 MHz)
- Programmable Real-Time Counter (RTC)
- 6 Clock Conditioning Circuits (CCCs) with 2 Integrated PLLs
  - Phase Shift, Multiply/Divide, and Delay Capabilities
  - Frequency: Input 1.5–350 MHz, Output 0.75–350 MHz

Low Power Consumption

- Single 3.3 V Power Supply with On-Chip 1.5 V Regulator
- Sleep and Standby Low-Power Modes

In-System Programming (ISP) and Security

- Secure ISP with 128-Bit AES via JTAG
- FlashLock® to Secure FPGA Contents

Advanced Digital I/O

- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages – Up to 5 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V /1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, M-LVDS
  - Built-In I/O Registers
  - 700 Mbps DDR Operation
- Hot-Swappable I/Os
- Programmable Output Slew Rate, Drive Strength, and Weak Pull-Up/Pull-Down Resistor
- Pin-Compatible Packages across the Fusion Family

SRAMs and FIFOs

- Variable-Aspect-Ratio 4,608-Bit SRAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)
- Programmable Embedded FIFO Control Logic

Soft ARM® Cortex™- M1 Fusion Devices (M1)

- ARM Cortex-M1–Enabled (without debug)

Table 1 • Fusion Extended Temperature Devices

Fusion Devices		AFS600	AFS1500
ARM Cortex-M1* Devices		M1AFS600	M1AFS1500
General Information	System Gates	600,000	1,500,000
	Tiles (D-flip-flops)	13,824	38,400
	Secure (AES) ISP	Yes	Yes
	PLLs	2	2
	Globals	18	18
Memory	Flash Memory Blocks (2 Mbits)	2	4
	Total Flash Memory Bits	4M	8M
	FlashROM Bits	1,024	1,024
	RAM Blocks (4,608 bits)	24	60
	RAM kbits	108	270
Analog and I/Os	Analog Quads	10	10
	Analog Input Channels	30	30
	Gate Driver Outputs	10	10
	I/O Banks (+ JTAG)	5	5
	Maximum Digital I/Os	172	252
	Analog I/Os	40	40

*Note: *Refer to the Cortex-M1 product brief for more information.*

† Refer to Table 2 on page IV for details.

Fusion Device Architecture Overview

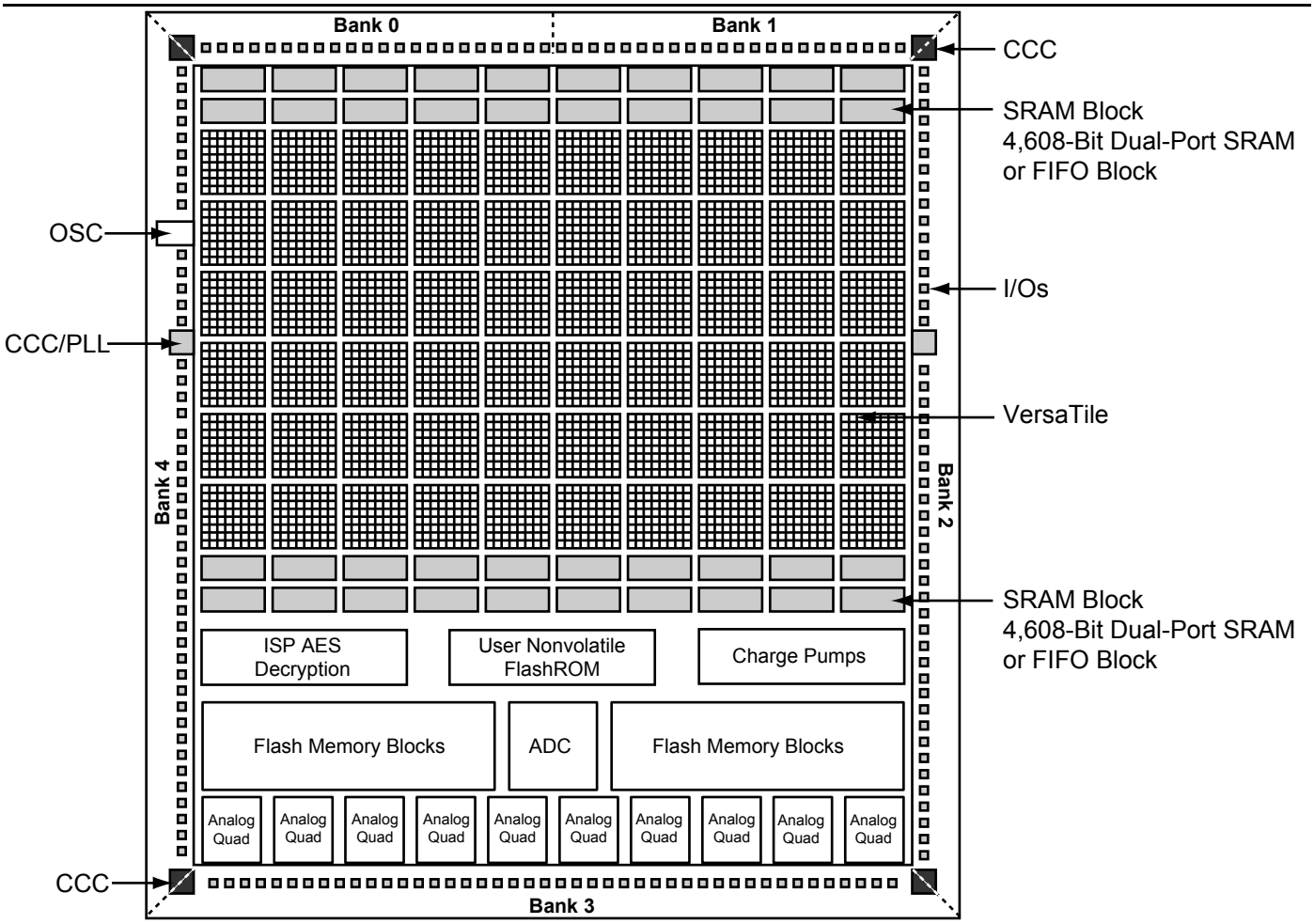
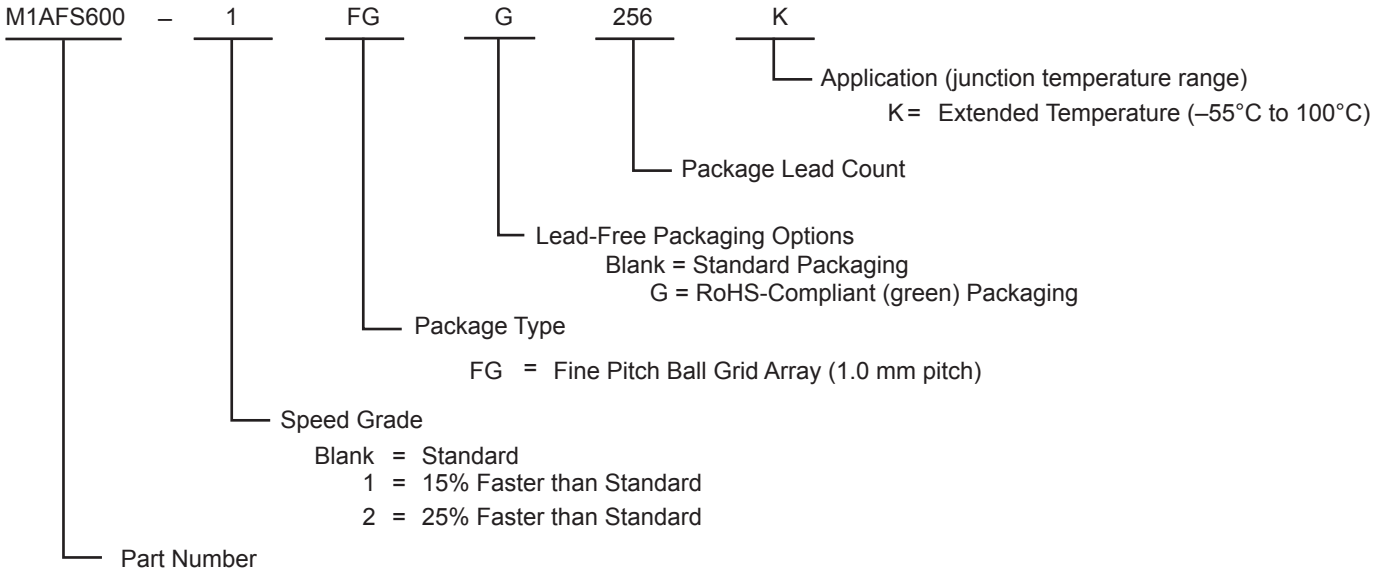


Figure 1 • **Fusion Device Architecture Overview (AFS600)**

Package I/Os: Single-/Double-Ended (Analog)

Fusion Devices	**AFS600**	**AFS1500**
ARM Cortex-M1 Devices	**M1AFS600**	**M1AFS1500**
FG256	119/58 (40)	119/58 (40)
FG484	172/86 (40)	223/109 (40)

Product Ordering Codes



Fusion Devices

AFS600 = 600,000 System Gates
AFS1500 = 1,500,000 System Gates

ARM-Enabled Fusion Devices

M1AFS600 = 600,000 System Gates
M1AFS1500 = 1,500,000 System Gates

Fusion Device Status

Fusion	Status	Cortex-M1	Status
AFS600	Production	M1AFS600	Production
AFS1500	Production	M1AFS1500	Production

Temperature Grade Offerings

Fusion Devices	AFS600	AFS1500
ARM Cortex-M1 Devices	**M1AFS600**	**M1AFS1500**
FG256	C, I, K	C, I, K
FG484	C, I, K	C, I, K

Notes:

1. *C = Commercial Temperature Range: 0°C to 85°C Junction. Refer to the commercial Fusion datasheet for details.*
2. *I = Industrial Temperature Range: –40°C to 100°C Junction. Refer to the commercial Fusion datasheet for details.*
3. *K = Extended Temperature Range: –55°C to 100°C Junction*

Speed Grade and Temperature Grade Matrix

	Std	–1	–2
K	✓	✓	✓

Note: K = Extended Temperature Range: –55°C to 100°C Junction

Summary of Differences Between Extended Temperature and Commercial/Industrial Grade Devices

Table 2 • Summary of Differences

Feature*	Extended Temperature	Commercial/Industrial Temperature
Temperature (junction)	–55°C to 100°C	0°C to 85°C / –40°C to 100°C
AV (negative voltage input)	Not supported between –40°C to –55°C	Supported across all temperatures
AC (positive voltage input)	Not supported between –40°C to –55°C	Supported across all temperatures
Sleep mode	Not supported between –40°C to –55°C	Supported across all temperatures
Pigeon Point ATCA IP support (P1)	Not Supported	Supported across all temperatures
MicroBlade Advanced Mezzanine Card support (U1)	Not Supported	Supported across all temperatures
Remainder of features	Supported across all temperatures	Supported across all temperatures

*Note: *This table lists only the differences in features. For additional details, refer to the "Device Architecture" section on page 2-1 and the "DC and Power Characteristics" section on page 3-1.*

Software Considerations for Extended Temperature Fusion

When designing with Actel Libero® integrated Design Environment (IDE) software, select the K package (example: 256 FBGA K) in the Device Selection Wizard. This enables the option of selecting the **EXT** temperature range under operating conditions.

Device Availability

Contact your local Actel representative for device availability (http://www.actel.com/contact/offices/index.html).

Table of Contents

1 – Fusion Device Family Overview

Introduction

The Actel Fusion® mixed signal FPGA satisfies the demand from system architects for a device that simplifies design and unleashes their creativity. As the world's first mixed signal programmable logic family, Fusion integrates mixed signal analog, flash memory, and FPGA fabric in a monolithic device. Actel Fusion devices enable designers to quickly move from concept to completed design and then deliver feature-rich systems to market. This new technology takes advantage of the unique properties of Actel flash-based FPGAs, including a high-isolation, triple-well process and the ability to support high-voltage transistors to meet the demanding requirements of mixed signal system design.

Actel Fusion mixed signal FPGAs bring the benefits of programmable logic to many application areas, including power management, smart battery charging, clock generation and management, and motor control. Until now, these applications have only been implemented with costly and space-consuming discrete analog components or mixed signal ASIC solutions. Actel Fusion mixed signal FPGAs present new capabilities for system development by allowing designers to integrate a wide range of functionality into a single device, while at the same time offering the flexibility of upgrades late in the manufacturing process or after the device is in the field. Actel Fusion devices provide an excellent alternative to costly and time-consuming mixed signal ASIC designs. In addition, when used in conjunction with the Actel Cortex-M1, Actel Fusion technology represents the definitive mixed signal FPGA platform.

Flash-based Fusion devices are live at power-up. As soon as the system power is applied, within normal operating specifications, Fusion devices start working. Fusion devices have a 128-bit flash-based lock and industry-leading AES decryption, used to secure programmed intellectual property (IP) and configuration data. Actel Fusion devices are the most comprehensive single-chip analog and digital programmable logic solution available today.

To support this new ground-breaking technology, Actel has developed a series of major tool innovations to help maximize designer productivity. Implemented as extensions to the popular Actel Libero® Integrated Design Environment (IDE), these new tools allow designers to easily instantiate and configure peripherals within a design, establish links between peripherals, create or import building blocks or reference designs, and perform hardware verification. This tool suite will also add comprehensive hardware/software debug capability as well as a suite of utilities to simplify development of embedded soft-processor-based solutions.

General Description

The Actel Fusion family, based on the highly successful ProASIC®3 and ProASIC3E flash FPGA architecture, has been designed as a high-performance, programmable, mixed signal platform. By combining an advanced flash FPGA core with flash memory blocks and analog peripherals, Fusion devices dramatically simplify system design and, as a result, dramatically reduce overall system cost and board space.

The state-of-the-art flash memory technology offers high-density integrated flash memory blocks, enabling savings in cost, power, and board area relative to external flash solutions, while providing increased flexibility and performance. The flash memory blocks and integrated analog peripherals enable true mixed-mode programmable logic designs. Two examples are using an on-chip soft processor to implement a fully functional flash microcontroller (MCU) and using high-speed FPGA logic to offer system and power supervisory capabilities. Live at power-up and capable of operating from a single 3.3 V supply, the Fusion family is ideally suited for system management and control applications.

The devices in the Fusion family are categorized by FPGA core density. The two family members contain many peripherals, including flash memory blocks, an analog-to-digital-converter (ADC), high-drive outputs, both RC and crystal oscillators, and a real-time counter (RTC). This provides the user with a high level of flexibility and integration to support a wide variety of mixed signal applications. The flash memory block capacity ranges from 4 Mbits to 8 Mbits. The integrated 12-bit ADC supports up to 30 independently configurable input channels. The on-chip crystal and RC oscillators work in conjunction

with the integrated phase-locked loops (PLLs) to provide clocking support to the FPGA array and on-chip resources. In addition to supporting typical RTC uses such as watchdog timer, the Fusion RTC can control the on-chip voltage regulator to power down the device (FPGA fabric, flash memory block, and ADC), enabling a low power standby mode.

The Actel Fusion family offers revolutionary features, never before available in an FPGA. The nonvolatile flash technology gives the Fusion solution the advantage of being a secure, low power, single-chip solution that is live at power-up. Fusion is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flash-based Fusion devices are live at power-up and do not need to be loaded from an external boot PROM. On-board security mechanisms prevent access to the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades, with confidence that valuable IP cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm with MAC data authentication on the device. The Fusion family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the Fusion family a cost-effective ASIC replacement solution for applications in the consumer, networking and communications, computing, and avionics markets.

Security

As the nonvolatile, flash-based Fusion family requires no boot PROM, there is no vulnerable external bitstream. Fusion devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Fusion devices utilize a 128-bit flash-based key lock and a separate AES key to secure programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the industry-leading AES-128 block cipher encryption standard (FIPS Publication 192). The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the DES standard, which was adopted in 1977. Fusion devices have a built-in AES decryption engine and a flash-based AES key that make Fusion devices the most comprehensive programmable logic device security solution available today. Fusion devices with AES-based security allow for secure remote field updates over public networks, such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the Fusion family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. Fusion with FlashLock and AES security is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected, making secure remote ISP possible. A Fusion device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Fusion FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

Flash-based Fusion devices are Level 0 live at power-up (LAPU). LAPU Fusion devices greatly simplify total system design and reduce total system cost by eliminating the need for CPLDs. The Fusion LAPU clocking (PLLs) replaces off-chip clocking resources. The Fusion mix of LAPU clocking and analog resources makes these devices an excellent choice for both system supervisor and system management functions. LAPU from a single 3.3 V source enables Fusion devices to initiate, control, and monitor multiple voltage supplies while also providing system clocks. In addition, glitches and brownouts in system power will not corrupt the Fusion device flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design. Flash-based Fusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. Another source of radiation-induced firm errors is alpha particles. For an alpha to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in Fusion flash-based FPGAs. Once it is programmed, the flash cell configuration element of Fusion FPGAs cannot be altered by high-energy neutrons and is therefore immune to errors from them.

Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With Fusion devices, there is no power-on current surge and no high current transition, both of which occur on many FPGAs.

Fusion devices also have low dynamic power consumption and support both low power standby mode and very low power sleep mode, offering further power savings.

Advanced Flash Technology

The Fusion family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows very high logic utilization (much higher than competing SRAM technologies) without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary Fusion architecture provides granularity comparable to standard-cell ASICs. The Fusion device consists of several distinct and programmable architectural features, including the following (Figure 1-1 on page 1-5):

- Embedded memories
  - Flash memory blocks
  - FlashROM
  - SRAM and FIFO

- Clocking resources
  - PLL and CCC
  - RC oscillator
  - Crystal oscillator
  - No-Glitch MUX (NGMUX)
- Digital I/Os with advanced I/O standards
- FPGA VersaTiles
- Analog components
  - ADC
  - Analog I/Os supporting voltage, current, and temperature monitoring[1]
  - 1.5 V on-board voltage regulator
  - Real-time counter

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic lookup table (LUT) equivalent or a D-flip-flop or latch (with or without enable) by programming the appropriate flash switch interconnections. This versatility allows efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel families of flash-based FPGAs. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid (3.3 V) single-voltage programming of Fusion devices via an IEEE 1532 JTAG interface.

Unprecedented Integration

Integrated Analog Blocks and Analog I/Os

Fusion devices offer robust and flexible analog mixed signal capability in addition to the high-performance flash FPGA fabric and flash memory block. The many built-in analog peripherals include a configurable 32:1 input analog MUX, up to 10 independent MOSFET gate driver outputs, and a configurable ADC. The ADC supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (Ksps), differential nonlinearity (DNL) less than 1.0 LSB, and total unadjusted error (TUE) of 0.72 LSB in 10-bit mode. The TUE is used for characterization of the conversion error and includes errors from all sources, such as offset and linearity. Internal bandgap circuitry offers 1% voltage reference accuracy with the flexibility of utilizing an external reference voltage. The ADC channel sampling sequence and sampling rate are programmable and implemented in the FPGA logic using Designer and Libero IDE software tool support.

Two channels of the 32-channel ADC MUX are dedicated. Channel 0 is connected internally to VCC and can be used to monitor core power supply. Channel 31 is connected to an internal temperature diode which can be used to monitor device temperature. The 30 remaining channels can be connected to external analog signals. The exact number of I/Os available for external connection signals is device-dependent (refer to Table 1 on page I for details).

With Fusion, Actel also introduces the Analog Quad I/O structure (Figure 1-1 on page 1-5). Each quad consists of three analog inputs and one gate driver. Each quad can be configured in various built-in circuit combinations, such as three prescaler circuits, three digital input circuits, a current monitor circuit, or a temperature monitor circuit. Each prescaler has multiple scaling factors programmed by FPGA signals to support a large range of analog inputs with positive or negative polarity. When the current monitor circuit is selected, two adjacent analog inputs measure the voltage drop across a small external sense resistor. For more information, refer to the "Analog System Characteristics" section on page 2-114 for more information. Built-in operational amplifiers amplify small voltage signals for accurate current measurement. One analog input in each quad can be connected to an external temperature monitor

1. *For additional details, refer to the "Device Architecture" section on page 2-1 and the "DC and Power Characteristics" section on page 3-1.*

diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADC MUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.

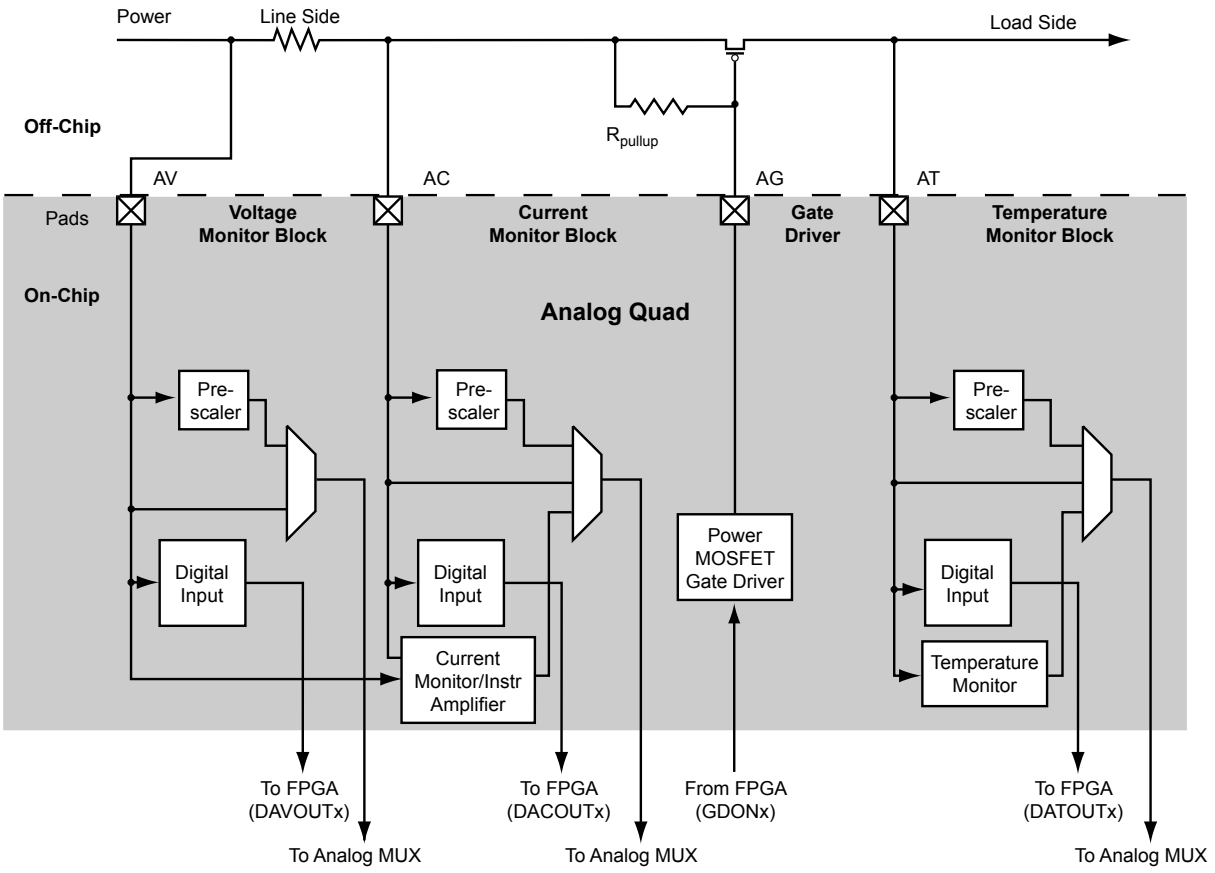


Figure 1-1 • **Analog Quad**

Embedded Memories

Flash Memory Blocks

The flash memory available in each Fusion device is composed of two to four flash blocks, each 2 Mbits in density. Each block operates independently with a dedicated flash controller and interface. Fusion flash memory blocks combine fast access times (60 ns random access and 10 ns access in Read-Ahead mode) with a configurable 8-, 16-, or 32-bit datapath, enabling high-speed flash operation without wait states. The memory block is organized in pages and sectors. Each page has 128 bytes, with 33 pages comprising one sector and 64 sectors per block. The flash block can support multiple partitions. The only constraint on size is that partition boundaries must coincide with page boundaries. The flexibility and granularity enable many use models and allow added granularity in programming updates.

Fusion devices support two methods of external access to the flash memory blocks. The first method is a serial interface that features a built-in JTAG-compliant port, which allows in-system programmability during user or monitor/test modes. This serial interface supports programming of an AES-encrypted stream. Secure data can be passed through the JTAG interface, decrypted, and then programmed in the flash block. The second method is a soft parallel interface.

FPGA logic or an on-chip soft microprocessor can access flash memory through the parallel interface. Since the flash parallel interface is implemented in the FPGA fabric, it can potentially be customized to meet special user requirements. For more information, refer to the *CoreCFI Handbook.* The flash memory parallel interface provides configurable byte-wide (×8), word-wide (×16), or dual-word-wide (×32) data port options. Through the programmable flash parallel interface, the on-chip and off-chip memories can be cascaded for wider or deeper configurations.

The flash memory has built-in security. The user can configure either the entire flash block or the small blocks to prevent unintentional or intrusive attempts to change or destroy the storage contents. Each on-chip flash memory block has a dedicated controller, enabling each block to operate independently.

The flash block logic consists of the following sub-blocks:

- Flash block – Contains all stored data. The flash block contains 64 sectors and each sector contains 33 pages of data.
- Page Buffer – Contains the contents of the current page being modified. A page contains 8 blocks of data.
- Block Buffer – Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic – The flash memory stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

User Nonvolatile FlashROM

In addition to the flash blocks, Actel Fusion devices have 1 Kbit of user-accessible, nonvolatile FlashROM on-chip. The FlashROM is organized as 8×128-bit pages. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IEEE 1532 JTAG programming interface. Pages can be individually programmed (erased and written). On-chip AES decryption can be used selectively over public networks to securely load data such as security keys stored in the FlashROM for a user design.

The FlashROM can be programmed (erased and written) via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing.

The FlashPoint tool in the Actel Fusion development software solutions, Libero IDE and Designer, has extensive support for flash memory blocks and FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

Fusion devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be written through a 4-bit port and read as a single bitstream. The SRAM blocks can be initialized from the flash memory blocks or via the device JTAG port (ROM emulation mode), using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and

Almost Full (AFULL) flags in addition to the normal EMPTY and FULL flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The SRAM/FIFO blocks can be cascaded to create larger configurations.

Clock Resources

PLLs and Clock Conditioning Circuits (CCCs)

Fusion devices provide designers with very flexible clock conditioning capabilities. Each member of the Fusion family contains six CCCs. For the Extended Temperature family, two of these CCCs also include a PLL.

The inputs of the CCC blocks are accessible from the FPGA core or from one of several inputs with dedicated CCC block connections.

The CCC block has the following key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock phase adjustment via programmable and fixed delays from –6.275 ns to +8.75 ns
- Clock skew minimization (PLL)
- Clock frequency synthesis (PLL)
- On-chip analog clocking resources usable as inputs:
  - 100 MHz on-chip RC oscillator
  - Crystal oscillator

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°
- Output duty cycle = 50% ± 1.5%
- Low output jitter. Samples of peak-to-peak period jitter when a single global network is used:
  - 70 ps at 350 MHz
  - 90 ps at 100 MHz
  - 180 ps at 24 MHz
  - Worst case < 2.5% × clock period
- Maximum acquisition time = 150 µs
- Low power consumption of 5 mW

Global Clocking

Fusion devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there are on-chip oscillators as well as a comprehensive global clock distribution network.

The integrated RC oscillator generates a 100 MHz clock. It is used internally to provide a known clock source to the flash memory read and write control. It can also be used as a source for the PLLs.

The crystal oscillator supports the following operating modes:

- Crystal (32.768 KHz to 20 MHz)
- Ceramic (500 KHz to 8 MHz)
- RC (32.768 KHz to 4 MHz)

Each VersaTile input and output port has access to nine VersaNets: six main and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via MUXes. The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Digital I/Os with Advanced I/O Standards

The Fusion family of FPGAs features a flexible digital I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Fusion FPGAs support many different digital I/O standards, both single-ended and differential.

The I/Os are organized into banks, with four or five banks per device. The configuration of these banks determines the I/O standards supported. The banks along the east and west sides of the device support the full range of I/O standards (single-ended and differential). The south bank supports the Analog Quads (analog I/O). This family of devices, the north bank supports multiple single-ended digital I/O standards. In the family's larger devices, the north bank is divided into two banks of digital Pro I/Os, supporting a wide variety of single-ended, differential, and voltage-referenced I/O standards.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following applications:

- Single-Data-Rate (SDR) applications
- Double-Data-Rate (DDR) applications—DDR LVDS I/O for chip-to-chip communications
- Fusion banks support LVPECL, LVDS, B-LVDS, and M-LVDS with 20 multi-drop points.

VersaTiles

The Fusion core consists of VersaTiles, which are also used in the successful Actel ProASIC3 family. The Fusion VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set and optional enable

Refer to Figure 1-2 for the VersaTile configuration arrangement.

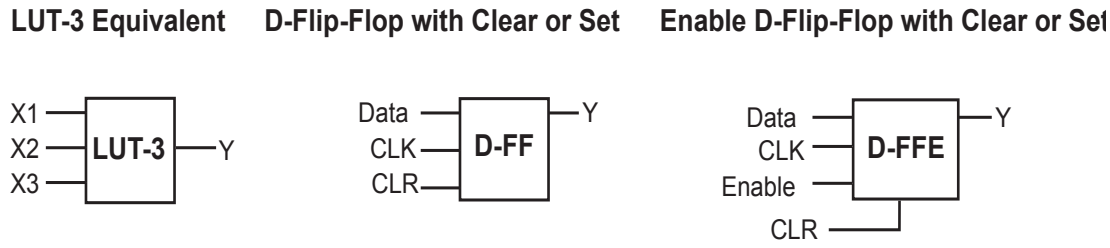


Figure 1-2 • **VersaTile Configurations**

Related Documents

Datasheet

Core8051
www.actel.com/ipdocs/Core8051_DS.pdf

Application Notes

Fusion FlashROM
http://www.actel.com/documents/Fusion_FROM_AN.pdf
Fusion SRAM/FIFO Blocks
http://www.actel.com/documents/Fusion_RAM_FIFO_AN.pdf
Using DDR in Fusion Devices
http://www.actel.com/documents/Fusion_DDR_AN.pdf
Fusion Security
http://www.actel.com/documents/Fusion_Security_AN.pdf
Using Fusion RAM as Multipliers
http://www.actel.com/documents/Fusion_Multipliers_AN.pdf

Handbook

Cortex-M1 Handbook
www.actel.com/documents/CortexM1_HB.pdf

User's Guides

Designer User's Guide
http://www.actel.com/documents/designer_UG.pdf
Fusion FPGA Fabric User's Guide
http://www.actel.com/documents/Fusion_UG.pdf
IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide
http://www.actel.com/documents/pa3_libguide_ug.pdf
SmartGen, FlashROM, Flash Memory System Builder, and Analog System Builder User's Guide
http://www.actel.com/documents/genguide_ug.pdf

White Papers

Fusion Technology
http://www.actel.com/documents/Fusion_Tech_WP.pdf

2 – Device Architecture

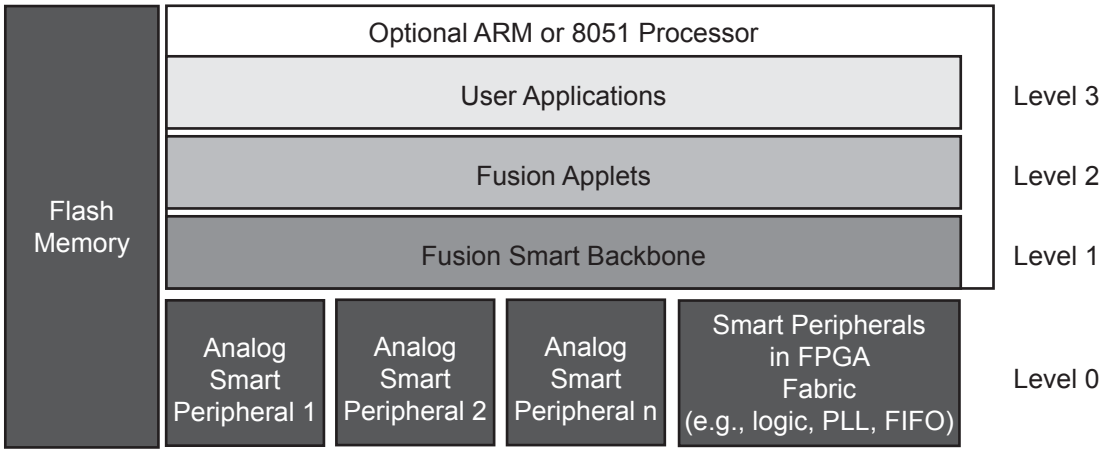
Fusion Stack Architecture

To manage the unprecedented level of integration in Fusion devices, Actel developed the Fusion technology stack (Figure 2-1). This layered model offers a flexible design environment, enabling design at very high and very low levels of abstraction. Fusion peripherals include hard analog IP and hard and soft digital IP. Peripherals communicate across the FPGA fabric via a layer of soft gates—the Fusion backbone. Much more than a common bus interface, this Fusion backbone integrates a micro-sequencer within the FPGA fabric and configures the individual peripherals and supports low-level processing of peripheral data. Fusion applets are application building blocks that can control and respond to peripherals and other system signals. Applets can be rapidly combined to create large applications. The technology is scalable across devices, families, design types, and user expertise, and supports a well-defined interface for external IP and tool integration.

At the lowest level, Level 0, are Fusion peripherals. These are configurable functional blocks that can be hardwired structures such as a PLL or analog input channel, or soft (FPGA gate) blocks such as a UART or two-wire serial interface. The Fusion peripherals are configurable and support a standard interface to facilitate communication and implementation.

Connecting and controlling access to the peripherals is the Fusion backbone, Level 1. The backbone is a soft-gate structure, scalable to any number of peripherals. The backbone is a bus and much more; it manages peripheral configuration to ensure proper operation. Leveraging the common peripheral interface and a low-level state machine, the backbone efficiently offloads peripheral management from the system design. The backbone can set and clear flags based upon peripheral behavior and can define performance criteria. The flexibility of the stack enables a designer to configure the silicon, directly bypassing the backbone if that level of control is desired.

One step up from the backbone is the Fusion applet, Level 2. The applet is an application building block that implements a specific function in FPGA gates. It can react to stimuli and board-level events coming through the backbone or from other sources, and responds to these stimuli by accessing and manipulating peripherals via the backbone or initiating some other action. An applet controls or responds to the peripheral(s). Applets can be easily imported or exported from the design environment. The applet structure is open and well-defined, enabling users to import applets from Actel, system developers, third parties, and user groups.



Note: Levels 1, 2, and 3 are implemented in FPGA logic gates.

Figure 2-1 • **Fusion Architecture Stack**

The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Actel Fusion technology stack, the application can be easily created in FPGA gates by importing and configuring multiple applets.

In fact, in some cases an entire FPGA system design can be created without any HDL coding.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Actel Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

Core Architecture

VersaTile

Based upon successful Actel ProASIC3/E logic architecture, Fusion devices provide granularity comparable to gate arrays. The Fusion device core consists of a sea-of-VersaTiles architecture.

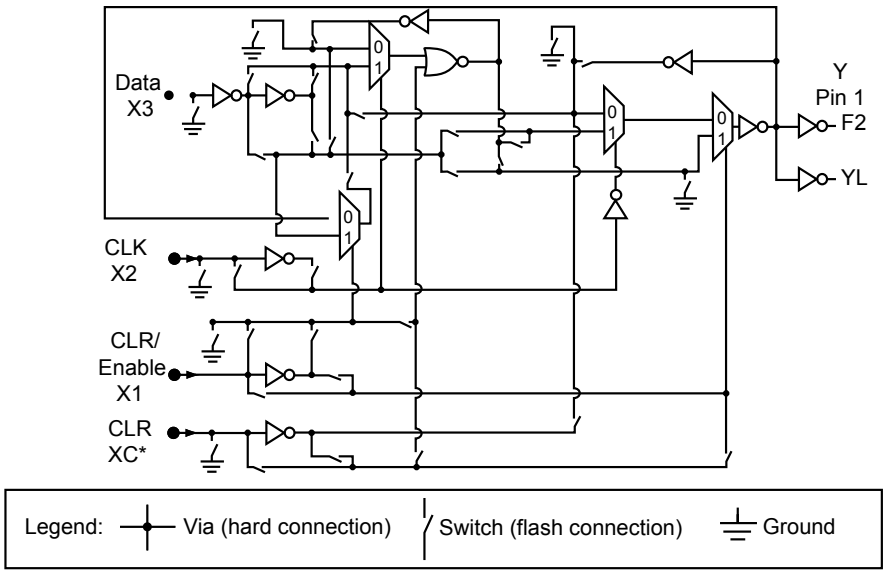
As illustrated in Figure 2-2, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet (global) network.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources (Figure 2-2).



*Note: *This input can only be connected to the global clock distribution network.*

Figure 2-2 • **Fusion Core VersaTile**

VersaTile Characteristics

Sample VersaTile Specifications—Combinatorial Module

The Fusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library (Figure 2-3). For more details, refer to the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide*.

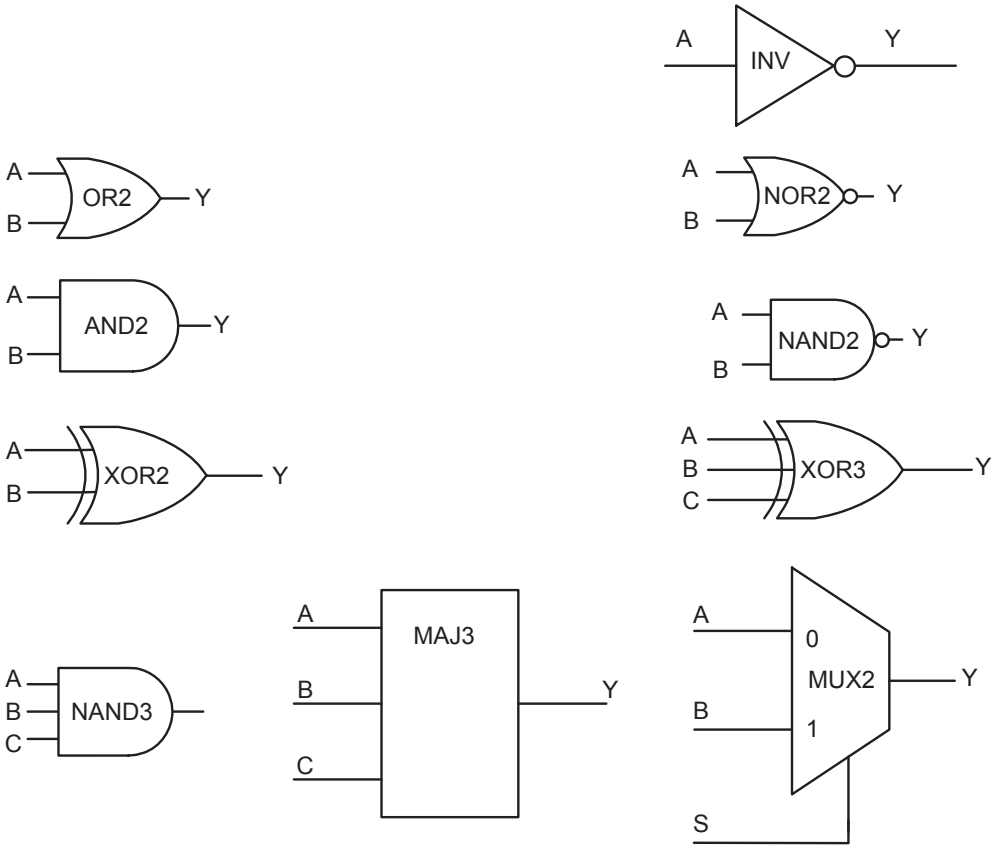


Figure 2-3 • **Sample of Combinatorial Cells**

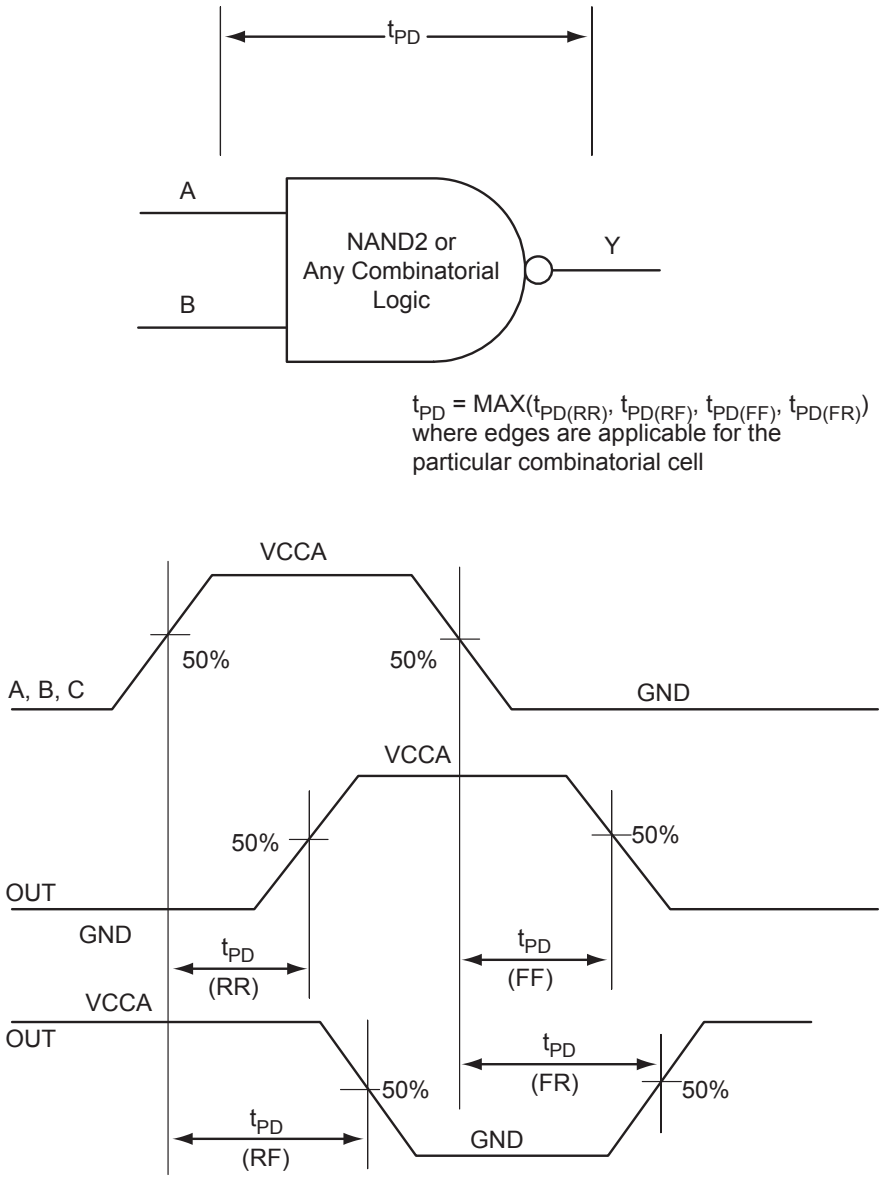


Figure 2-4 • **Combinatorial Timing Model and Waveforms**

Timing Characteristics

Table 2-1 • Combinatorial Cell Propagation Delays
Extended Temperature Range Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.47	0.55	ns
AND2	Y = A · B	t_{PD}	0.49	0.55	0.65	ns
NAND2	Y = !(A · B)	t_{PD}	0.49	0.55	0.65	ns
OR2	Y = A + B	t_{PD}	0.50	0.57	0.67	ns
NOR2	Y = !(A + B)	t_{PD}	0.50	0.57	0.67	ns
XOR2	Y = A ⊕ B	t_{PD}	0.76	0.87	1.02	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.72	0.82	0.96	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.90	1.03	1.21	ns
MUX2	Y = A !S + B S	t_{PD}	0.52	0.60	0.70	ns
AND3	Y = A · B · C	t_{PD}	0.58	0.66	0.77	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Sample VersaTile Specifications—Sequential Module

The Fusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library (Figure 2-5). For more details, refer to the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide*.

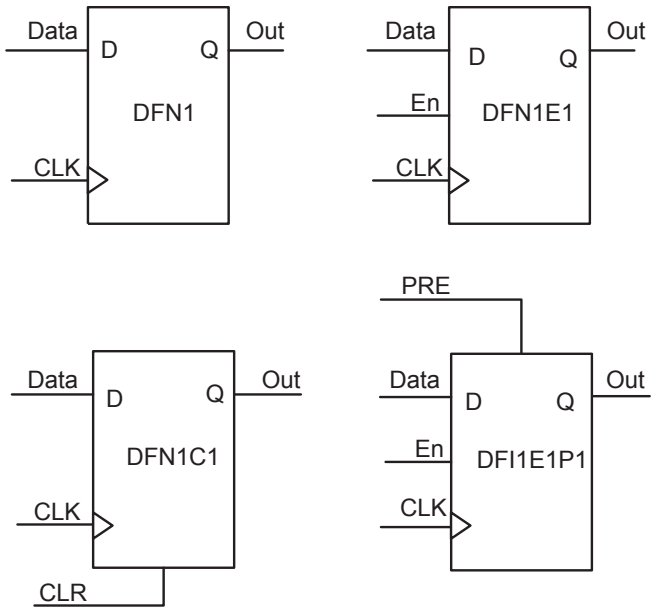


Figure 2-5 • Sample of Sequential Cells

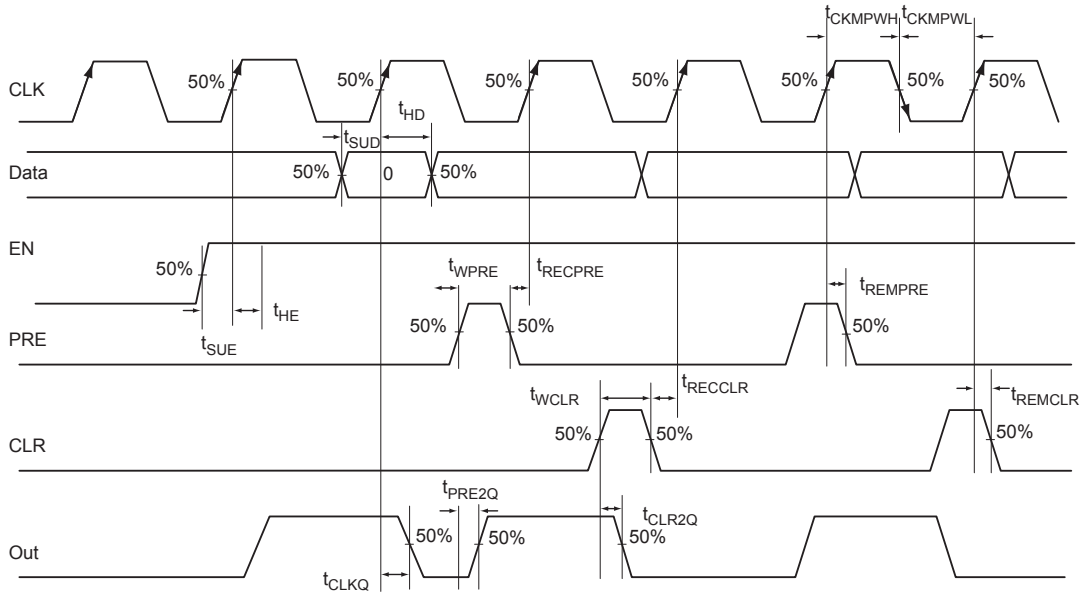


Figure 2-6 • **Sequential Timing Model and Waveforms**

Sequential Timing Characteristics

Table 2-2 • **Register Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.57	0.65	0.76	ns
t_{SUD}	Data Setup Time for the Core Register	0.44	0.50	0.59	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.47	0.53	0.63	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.41	0.47	0.55	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.41	0.47	0.55	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.23	0.26	0.31	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	0.26	0.31	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.37	0.43	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.41	0.48	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Array Coordinates

During many place-and-route operations in the Actel Designer software tool, it is possible to set constraints that require array coordinates. Table 2-3 is provided as a reference. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

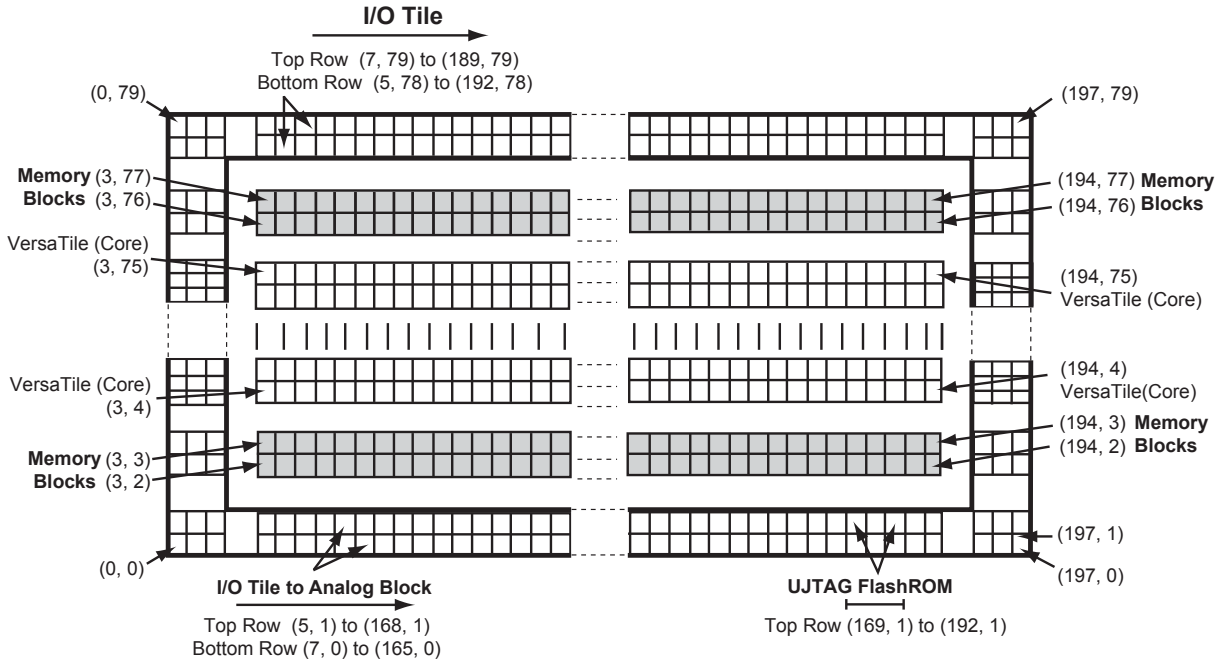
Table 2-3 provides array coordinates of core cells and memory blocks.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and edge core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-3. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-7 illustrates the array coordinates of an AFS600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for Fusion software tools.

Table 2-3 • **Array Coordinates**

Device	VersaTiles				Memory Rows		All	
	Min.		Max.		Bottom	Top	Min.	Max.
	x	y	x	y	(x, y)	(x, y)	(x, y)	(x, y)
AFS600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)
AFS1500	3	4	322	123	(3, 2)	(3, 124)	(0, 0)	(325, 129)



Note: The vertical I/O tile coordinates are not shown. West side coordinates are {(0, 2) to (2, 2)} to {(0, 77) to (2, 77)}; east side coordinates are {(195, 2) to (197, 2)} to {(195, 77) to (197, 77)}.

Figure 2-7 • **Array Coordinates for AFS600**

Routing Architecture

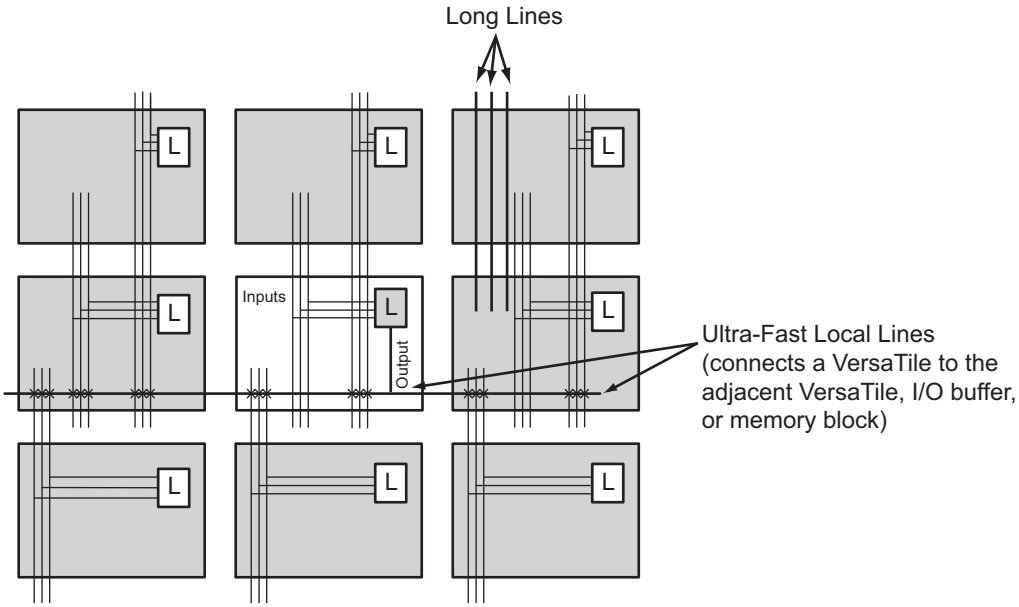
The routing structure of Fusion devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources; efficient long-line resources; high-speed very-long-line resources; and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 2-8). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaNet global network.

The efficient long-line resources provide routing for longer distances and higher-fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire Fusion device (Figure 2-9 on page 2-9). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Active buffers are inserted automatically by routing software to limit loading effects.

The high-speed very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length ±12 VersaTiles in the vertical direction and length ±16 in the horizontal direction from a given core VersaTile (Figure 2-10 on page 2-10). Very long lines in Fusion devices, like those in ProASIC3 devices, have been enhanced. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or from internal logic (Figure 2-11 on page 2-11). These nets are typically used to distribute clocks, reset signals, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all VersaTiles.



Note: Input to the core cell for the D-flip-flop set and reset is only available via the VersaNet global network connection.

Figure 2-8 • **Ultra-Fast Local Lines Connected to the Eight Nearest Neighbors**

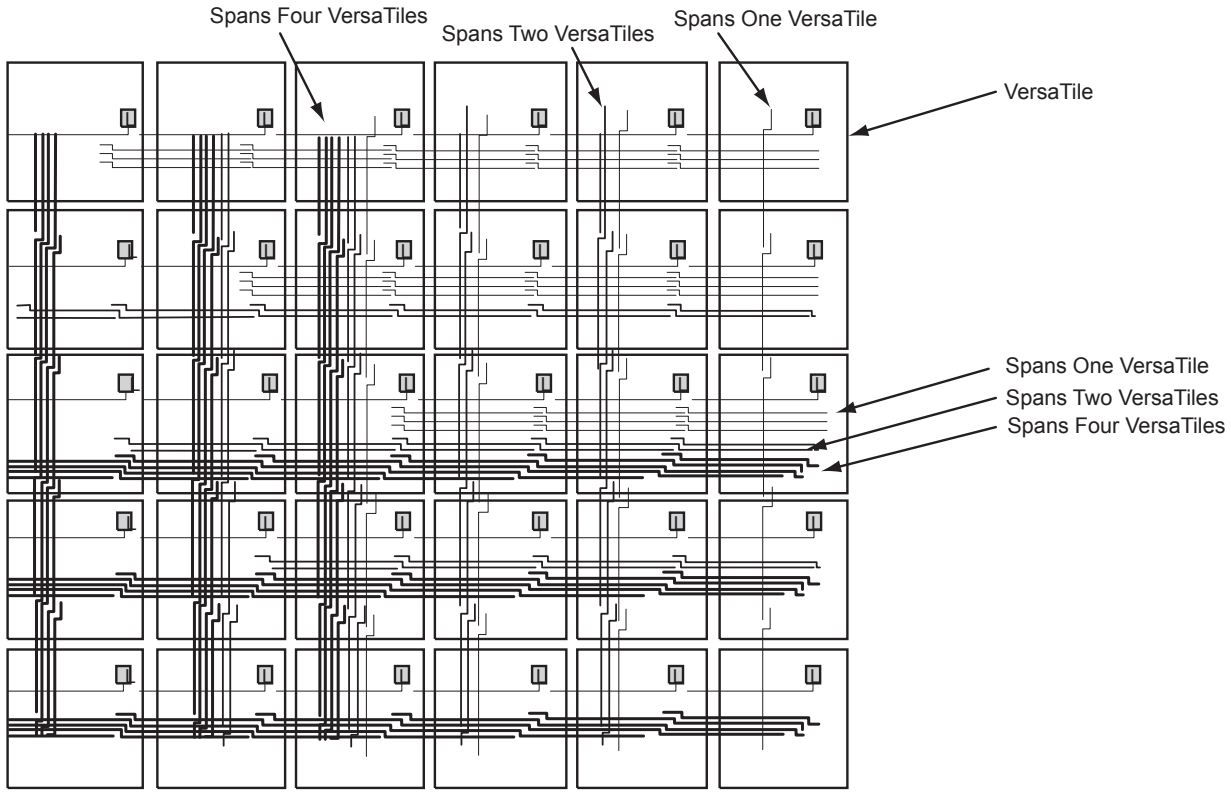


Figure 2-9 • **Efficient Long-Line Resources**

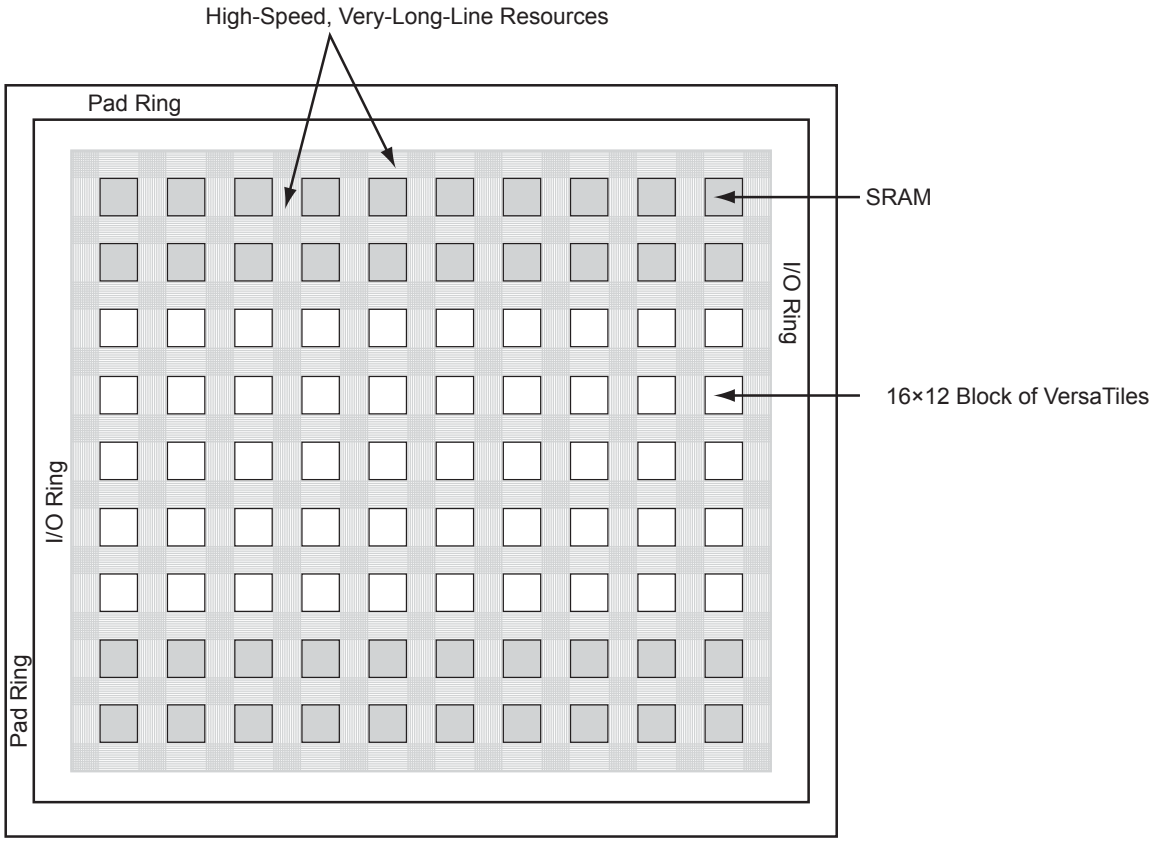


Figure 2-10 • **Very-Long-Line Resources**

Global Resources (VersaNets)

Fusion devices offer powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has six CCCs. The west CCC also contains a PLL core. In the AFS600 and AFS1500, the west and the east CCCs each contain a PLL. The PLLs include delay lines, a phase shifter (0°, 90°, 180°, 270°), and clock multipliers/dividers. Each CCC has all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six lines total). The CCCs at the four corners each have access to three quadrant global lines on each quadrant of the chip.

Advantages of the VersaNet Approach

One of the architectural benefits of Fusion is the set of powerful and low-delay VersaNet global networks. Fusion offers six chip (main) global networks that are distributed from the center of the FPGA array (Figure 2-11). In addition, Fusion devices have three regional globals (quadrant globals) in each of the four chip quadrants. Each core VersaTile has access to nine global network resources: three quadrant and six chip (main) global networks. There are a total of 18 global networks on the device. Each of these networks contains spines and ribs that reach all VersaTiles in all quadrants (Figure 2-12 on page 2-12). This flexible VersaNet global network architecture allows users to map up to 180 different internal/external clocks in a Fusion device. Details on the VersaNet networks are given in Table 2-4 on page 2-12. The flexibility of the Fusion VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet global network.

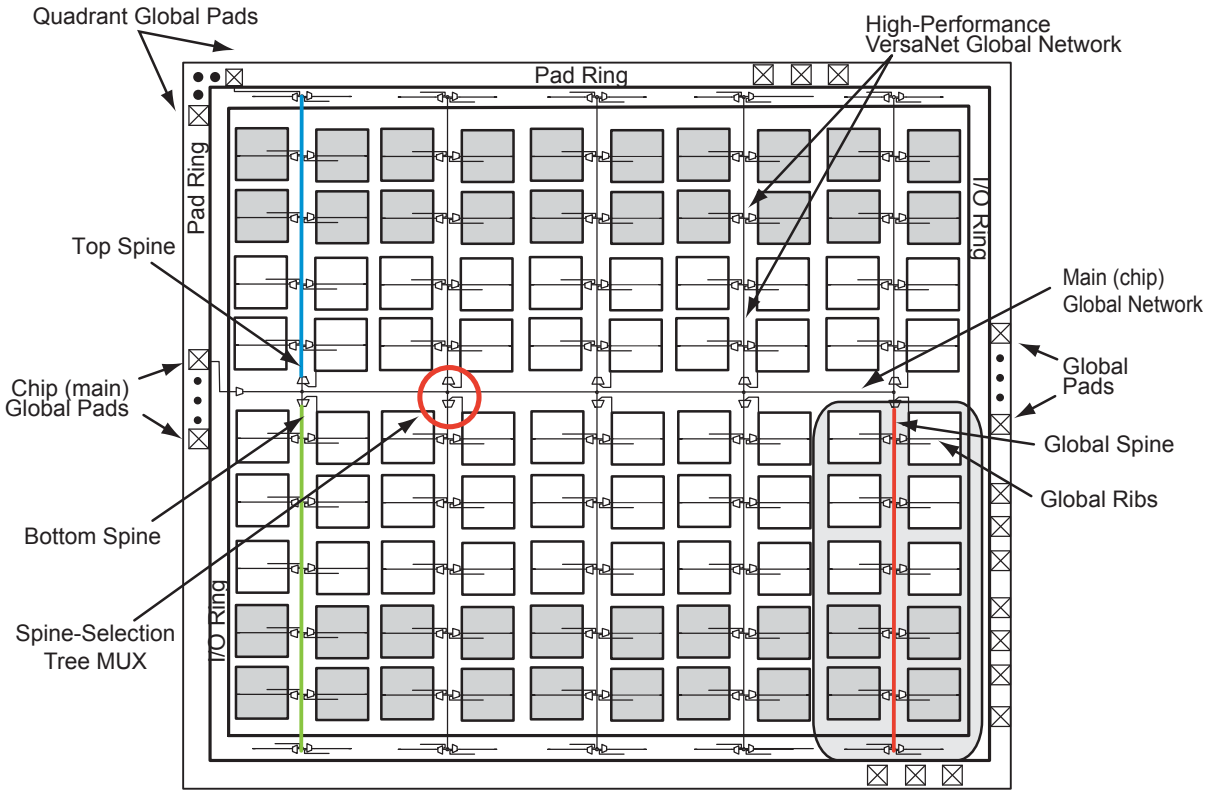


Figure 2-11 • **Overview of Fusion VersaNet Global Network**

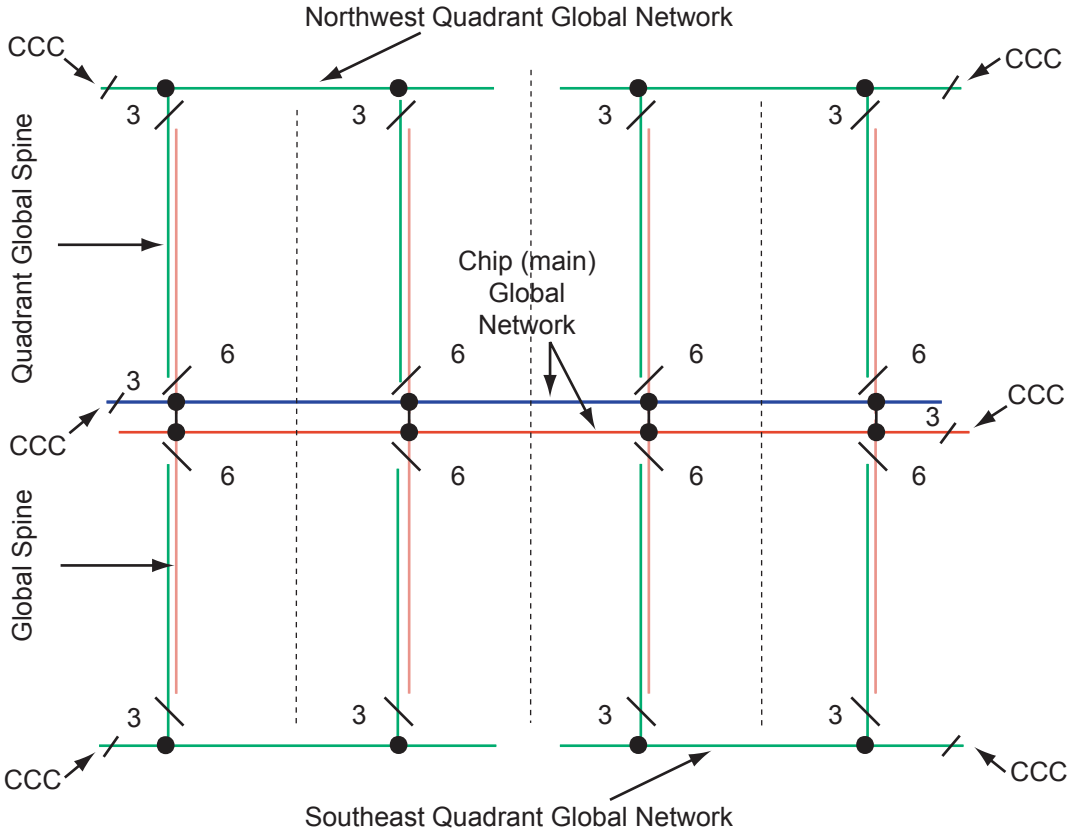


Figure 2-12 • **Global Network Architecture**

Table 2-4 • **Globals/Spines/Rows by Device**

	AFS600	AFS1500
Global VersaNets (trees)*	9	9
VersaNet Spines/Tree	12	20
Total Spines	108	180
VersaTiles in Each Top or Bottom Spine	1,152	1,920
Total VersaTiles	13,824	38,400

*Note: *There are six chip (main) globals and three globals per quadrant.*

VersaNet Global Networks and Spine Access

The Fusion architecture contains a total of 18 segmented global networks that can access the VersaTiles, SRAM, and I/O tiles on the Fusion device. There are 6 chip (main) global networks that access the entire device and 12 quadrant networks (3 in each quadrant). Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 180 internal/external clocks (in an AFS1500 device) or other high-fanout nets in Fusion devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on Fusion devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device. There are four quadrant global network regions per device (Figure 2-12 on page 2-12).

The spines are the vertical branches of the global network tree, shown in Figure 2-11 on page 2-11. Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the Fusion device (the "scope" of the spine; see Figure 2-11 on page 2-11). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or another net defined by the user (Figure 2-13). Quadrant spines can be driven from user I/Os on the north and south sides of the die, via analog I/Os configured as direct digital inputs. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 2-13. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device. For details on using spines in Fusion devices, see the Actel application note *Using Global Resources in Actel Fusion Devices*.

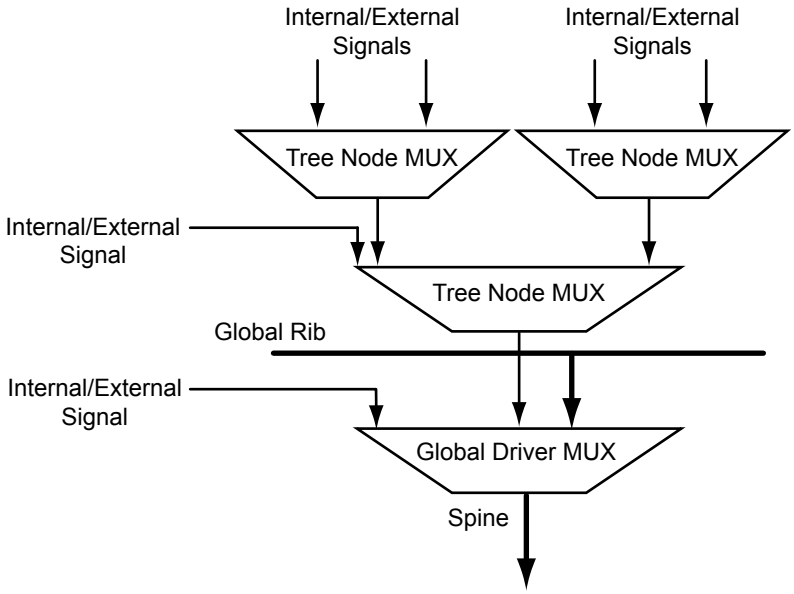


Figure 2-13 • **Spine-Selection MUX of Global Tree**

Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 2-14 indicates, this access system is contiguous.

There is no break in the middle of the chip for north and south I/O VersaNet access. This is different from the quadrant clocks, located in these ribs, which only reach the middle of the rib. Refer to the *Using Global Resources in Actel Fusion Devices* application note.

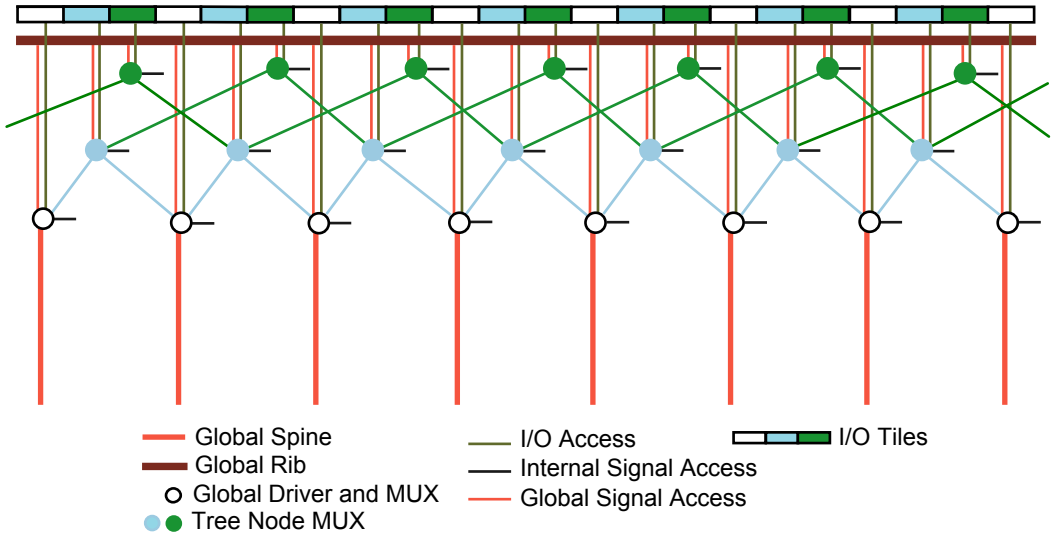


Figure 2-14 • **Clock Aggregation Tree Architecture**

Global Resource Characteristics

AFS600 VersaNet Topology

Clock delays are device-specific. Figure 2-15 is an example of a global tree used for clock routing. The global tree presented in Figure 2-15 is driven by a CCC located on the west side of the AFS600 device. It is used to drive all D-flip-flops in the device.

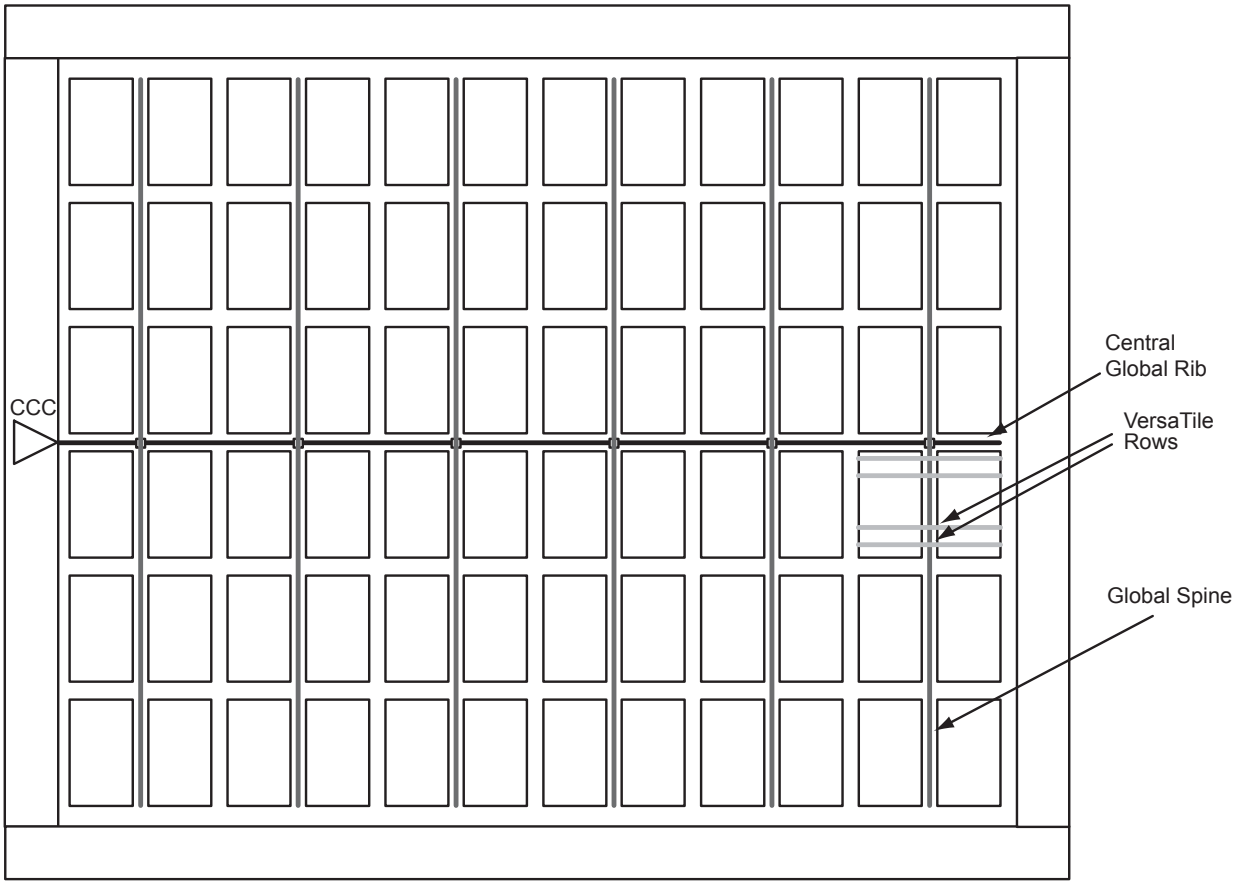


Figure 2-15 • **Example of Global Tree Use in an AFS600 Device for Clock Routing**

VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. Table 2-5 and Table 2-6 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading, respectively.

Timing Characteristics

Table 2-5 • AFS1500 Global Resource Timing, Extended Temperature Case Conditions: T_J = 100°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.59	1.81	1.81	2.06	2.12	2.43	ns
t_{RCKH}	Input High Delay for Global Clock	1.59	1.86	1.81	2.12	2.13	2.49	ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27		0.31		0.36	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.*

Table 2-6 • AFS600 Global Resource Timing, Extended Temperature Case Conditions: T_J = 100°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.31	1.55	1.49	1.76	1.76	2.08	ns
t_{RCKH}	Input High Delay for Global Clock	1.31	1.59	1.49	1.81	1.75	2.13	ns
t_{RCKSW}	Maximum Skew for Global Clock		0.28		0.32		0.38	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.*

Clocking Resources

The Fusion family has a robust collection of clocking peripherals, as shown in the block diagram in Figure 2-16. These on-chip resources enable the creation, manipulation, and distribution of many clock signals. The Fusion integrated RC oscillator produces a 100 MHz clock source with no external components. For systems requiring more precise clock signals, the Actel Fusion family supports an on-chip crystal oscillator circuit. The integrated PLLs in each Fusion device can use the RC oscillator, crystal oscillator, or another on-chip clock signal as a source. These PLLs offer a variety of capabilities to modify the clock source (multiply, divide, synchronize, advance, or delay). Utilizing the CCC found in the popular Actel ProASIC3 family, Fusion incorporates six CCC blocks. The CCCs allow access to Fusion global and local clock distribution nets, as described in the "Global Resources (VersaNets)" section on page 2-11.

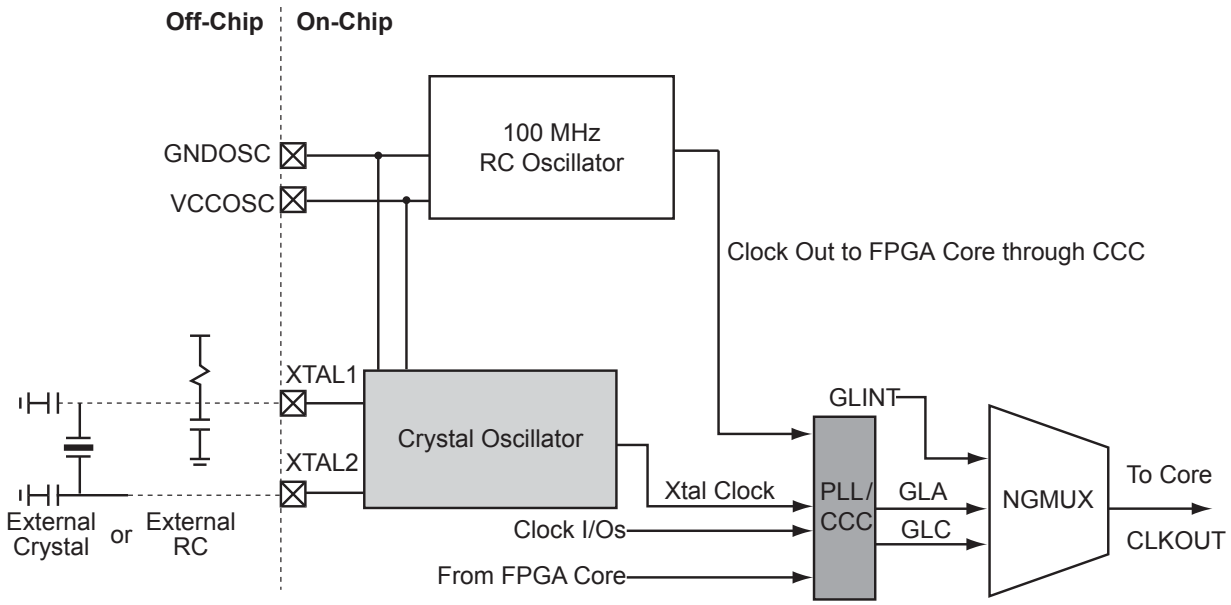


Figure 2-16 • **Fusion Clocking Options**

RC Oscillator

The RC oscillator is an on-chip free-running clock source generating a 100 MHz clock. It can be used as a source clock for both on-chip and off-chip resources. When used in conjunction with the Fusion PLL and CCC circuits, the RC oscillator clock source can be used to generate clocks of varying frequency and phase.

The Fusion RC oscillator is very accurate at ±1% over commercial and industrial temperature ranges. It is an automated clock, requiring no setup or configuration by the user. It requires only that the power and GNDOSC pins be connected; no external components are required. The RC oscillator can be used to drive either a PLL or another internal signal.

RC Oscillator Characteristics

Table 2-7 • Electrical Characteristics of RC Oscillator

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
FRC	Operating Frequency			100		MHz
	Accuracy	Temperature: 0°C to 85°C Voltage: 3.3 V ± 5%		1		%
		Temperature: –55°C to 100°C Voltage: 3.3 V ± 5%		3		%
	Output Jitter	Period Jitter (at 5 k cycles)		100		ps
		Cycle–Cycle Jitter (at 5 k cycles)		100		ps
		Period Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps
		Cycle–Cycle Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps
	Output Duty Cycle			50		%
I_{DYNRC}	Operating Current			1		mA

Crystal Oscillator

The Crystal Oscillator (XTLOSC) is source that generates the clock from an external crystal. The output of XTLOSC CLKOUT signal can be selected as an input to the PLL. Refer to "Clock Conditioning Circuits" section for more details. The XTLOSC can operate in normal operations and Standby mode (RTC is running and 1.5 V is not present).

In normal operation, the internal FPGA_EN signal is '1' as long as 1.5 V is present for VCC. As such, the internal enable signal, XTL_EN, for Crystal Oscillator is enabled since FPGA_EN is asserted. The XTL_MODE has the option of using MODE or RTC_MODE, depending on SELMODE.

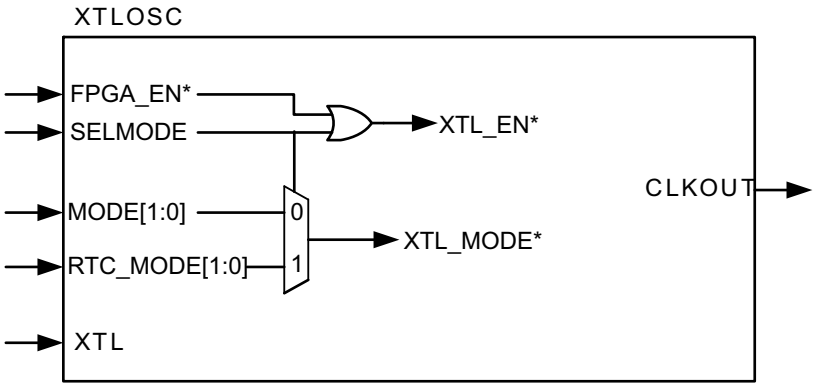
During Standby, 1.5 V is not available, as such, and FPGA_EN is '0'. SELMODE must be asserted in order for XTL_EN to be enabled; hence XTL_MODE relies on RTC_MODE. SELMODE and RTC_MODE must be connected to RTCXTLSEL and RTCXTLMODE from the AB respectively for correct operation during Standby (refer to the "Real-Time Counter System" section on page 2-31 for a detailed description).

The Crystal Oscillator can be configured in one of four modes:

- RC network, 32 KHz to 4 MHz
- Low gain, 32 to 200 KHz
- Medium gain, 0.20 to 2.0 MHz
- High gain, 2.0 to 20.0 MHz

In RC network mode, the XTAL1 pin is connected to an RC circuit, as shown in Figure 2-17. The XTAL2 pin should be left floating. The RC value can be chosen based on Figure 2-18 for any desired frequency between 32 KHz and 4 MHz. The RC network mode can also accommodate an external clock source on XTAL1 instead of an RC circuit.

In Low gain, Medium gain, and High gain, an external crystal component or ceramic resonator can be added onto XTAL1 and XTAL2, as shown in Figure 2-17.



*Note: *Internal signal—does not exist in macro.*

Figure 2-17 • **XTLOSC Macro**

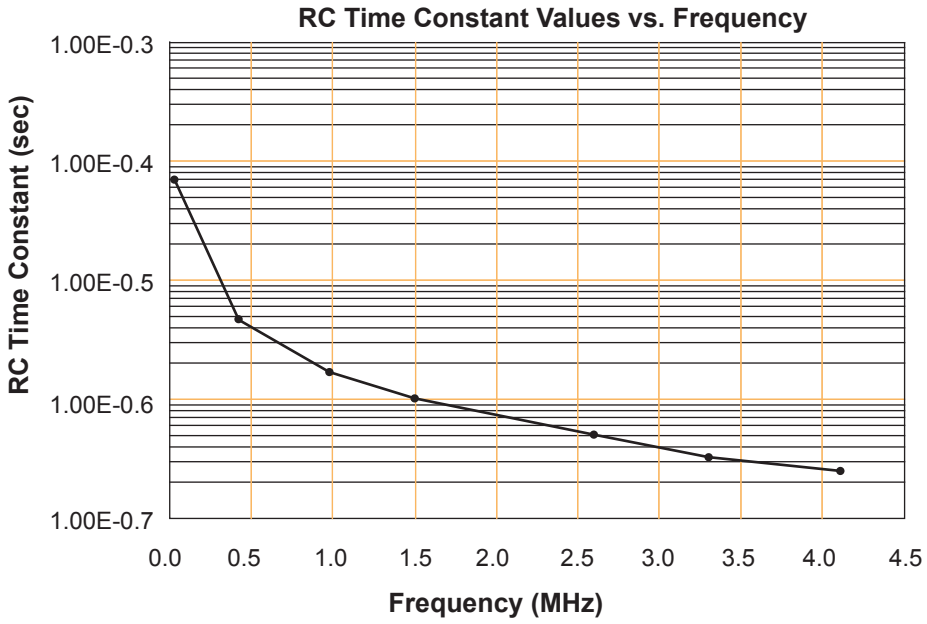


Figure 2-18 • **Crystal Oscillator: RC Time Constant Values vs. Frequency (typical)**

Table 2-8 • **XTLOSC Signals Descriptions**

Signal Name	Width	Direction	Function
XTL_EN*	1		Enables the crystal. Active high.
XTL_MODE*	2		Settings for the crystal clock for different frequency. **Value** / **Modes** / **Frequency Range** b'00 / RC network / 32 KHz to 4 MHz b'01 / Low gain / 32 to 200 KHz b'10 / Medium gain / 0.20 to 2.0 MHz b'11 / High gain / 2.0 to 20.0 MHz
SELMODE	1	IN	Selects the source of XTL_MODE and also enables the XTL_EN. Connect from RTCXTLSEL from AB. 0 For normal operation or sleep mode, XTL_EN depends on FPGA_EN, XTL_MODE depends on MODE 1 For Standby mode, XTL_EN is enabled, XTL_MODE depends on RTC_MODE
RTC_MODE[1:0]	2	IN	Settings for the crystal clock for different frequency ranges. XTL_MODE uses RTC_MODE when SELMODE is '1'.
MODE[1:0]	2	IN	Settings for the crystal clock for different frequency ranges. XTL_MODE uses MODE when SELMODE is '0'. In Standby, MODE inputs will be 0s.
FPGA_EN*	1	IN	0 when 1.5 V is not present for VCC 1 when 1.5 V is present for VCC
XTL	1	IN	Crystal Clock source
CLKOUT	1	OUT	Crystal Clock output

*Note: *Internal signal—does not exist in macro.*

Table 2-9 • **Electrical Characteristics of the Crystal Oscillator**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
FXTAL	Operating Frequency	Using External Crystal	0.032		20	MHz
		Using Ceramic Resonator	0.5		8	MHz
		Using RC Network	0.032		4	MHz
	Output Duty Cycle			50		%
	Output Jitter	With 10 MHz Crystal		50		ps RMS
IDYNXTAL	Operating Current	RC		0.6		mA
		0.032–0.2		0.6		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
ISTBXTAL	Standby Current			10		µA
PSRRXTAL	Power Supply Noise Tolerance			0.5		Vp-p
VIHXTAL	Input Logic Level High		90% of VCC			V
VILXTAL	Input Logic Level Low				10% of VCC	V

Clock Conditioning Circuits

In Fusion devices, the CCCs are used to implement frequency division, frequency multiplication, phase shifting, and delay operations.

The CCCs are available in six chip locations—each of the four chip corners and the middle of the east and west chip sides.

Each CCC can implement up to three independent global buffers (with or without programmable delay), or a PLL function (programmable frequency division/multiplication, phase shift, and delays) with up to three global outputs. Unused global outputs of a PLL can be used to implement independent global buffers, up to a maximum of three global outputs for a given CCC.

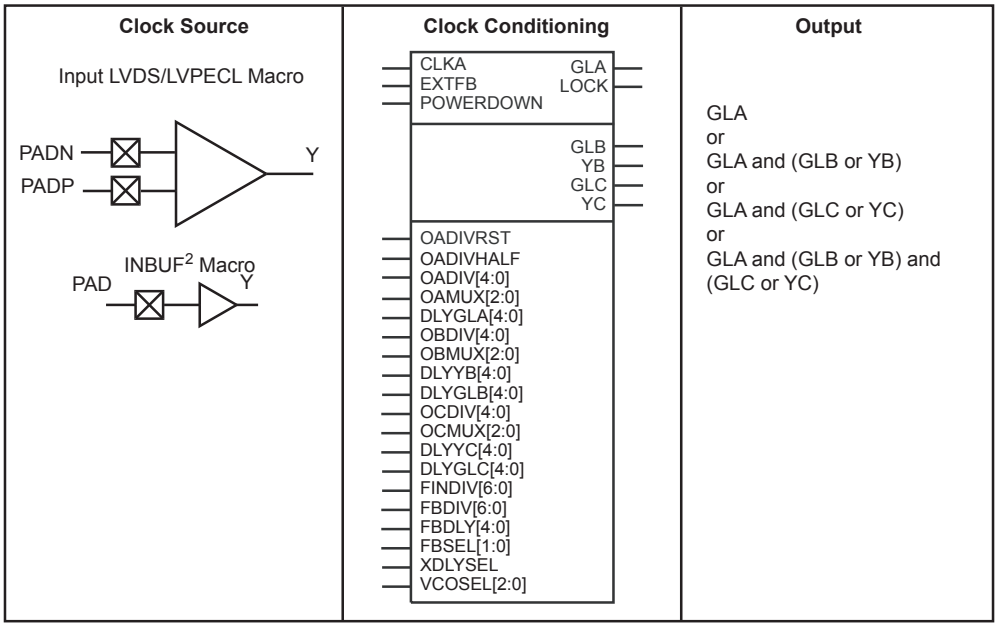
A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, and CLKC-GLC) of a given CCC.

A PLL macro uses the CLKA CCC input to drive its reference clock. It uses the GLA and, optionally, the GLB and GLC global outputs to drive the global networks. A PLL macro can also drive the YB and YC regular core outputs. The GLB (or GLC) global output cannot be reused if the YB (or YC) output is used (Figure 2-19). Refer to the "PLL Macro" section on page 2-27 for more information.

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core

The CCC block is fully configurable, either via flash configuration bits set in the programming bitstream or through an asynchronous interface. This asynchronous interface is dynamically accessible from inside the Fusion device to permit changes of parameters (such as divide ratios) during device operation. To increase the versatility and flexibility of the clock conditioning system, the CCC configuration is determined either by the user during the design process, with configuration data being stored in flash memory as part of the device programming procedure, or by writing data into a dedicated shift register during normal device operation. This latter mode allows the user to dynamically reconfigure the CCC without the need for core programming. The shift register is accessed through a simple serial interface. Refer to the "UJTAG Applications in Actel's Low-Power Flash Devices" chapter of the *Fusion FPGA Fabric User's Guide* and the "CCC and PLL Characteristics" section on page 2-28 for more information.



Notes:

1. *Visit the Actel website for future application notes concerning dynamic PLL reconfiguration. Refer to the "PLL Macro" section on page 2-27 for signal descriptions.*
2. *Many specific INBUF macros support the wide variety of single-ended and differential I/O standards for the Fusion family.*
3. *Refer to the IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide for more information.*

Figure 2-19 • **Fusion CCC Options: Global Buffers with the PLL Macro**

Table 2-10 • **Available Selections of I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros**

CLKBUF Macros
CLKBUF_LVCMOS5
CLKBUF_LVCMOS33[1]
CLKBUF_LVCMOS18
CLKBUF_LVCMOS15
CLKBUF_PCI
CLKBUF_LVDS[2]
CLKBUF_LVPECL

Notes:

1. *This is the default macro. For more details, refer to the IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide.*
2. *The B-LVDS and M-LVDS standards are supported with CLKBUF_LVDS.*

Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS macros are composite macros that include an I/O macro driving a global buffer, hardwired together (Figure 2-20).

The CLKINT macro provides a global buffer function driven by the FPGA core.

The CLKBUF, CLKBUF_LVPECL/LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by Fusion devices. The available CLKBUF macros are described in the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide*.

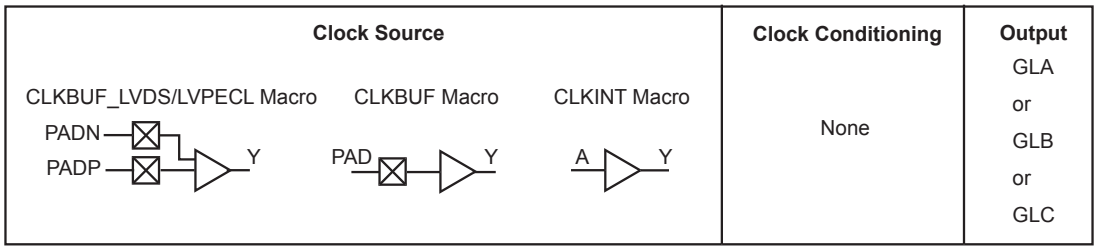


Figure 2-20 • **Global Buffers with No Programmable Delay**

Global Buffers with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay (Figure 2-21). The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

The CLKDLY macro can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the Fusion family. The available INBUF macros are described in the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide.*

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero IDE and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.

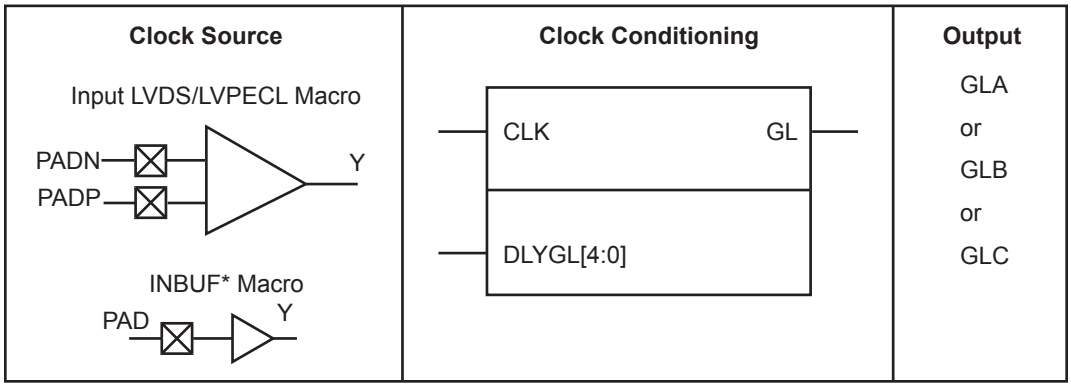
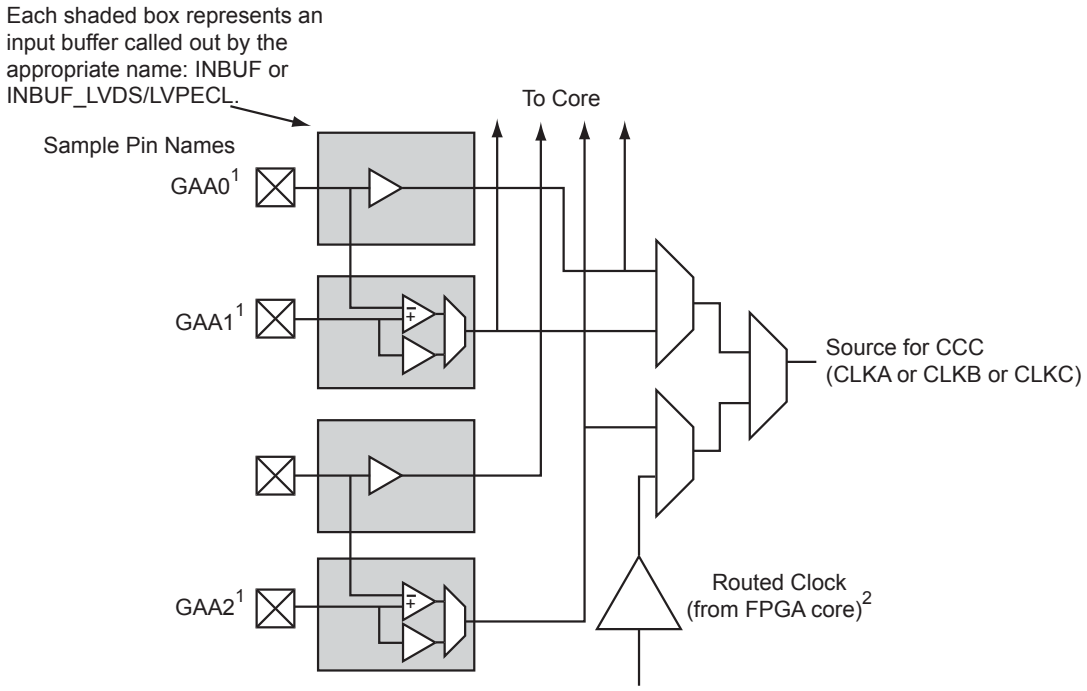


Figure 2-21 • **Fusion CCC Options: Global Buffers with Programmable Delay**

Global Input Selections

Each global buffer, as well as the PLL reference clock, can be driven from one of the following (Figure 2-22):

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core



GAA[0:2]: GA represents global in the northwest corner of the device. A[0:2]: designates specific A clock source.

Notes:

1. *Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to the "User I/O Naming Convention" section on page 2-156 for more information.*
2. *Instantiate the routed clock source input as follows:*
   a) Connect the output of a logic element to the clock input of the PLL, CLKDLY, or CLKINT macro.
   b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS) in a relevant global pin location.
3. *LVDS-based clock sources are available in the east and west banks on all Fusion devices.*

Figure 2-22 • **Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT**

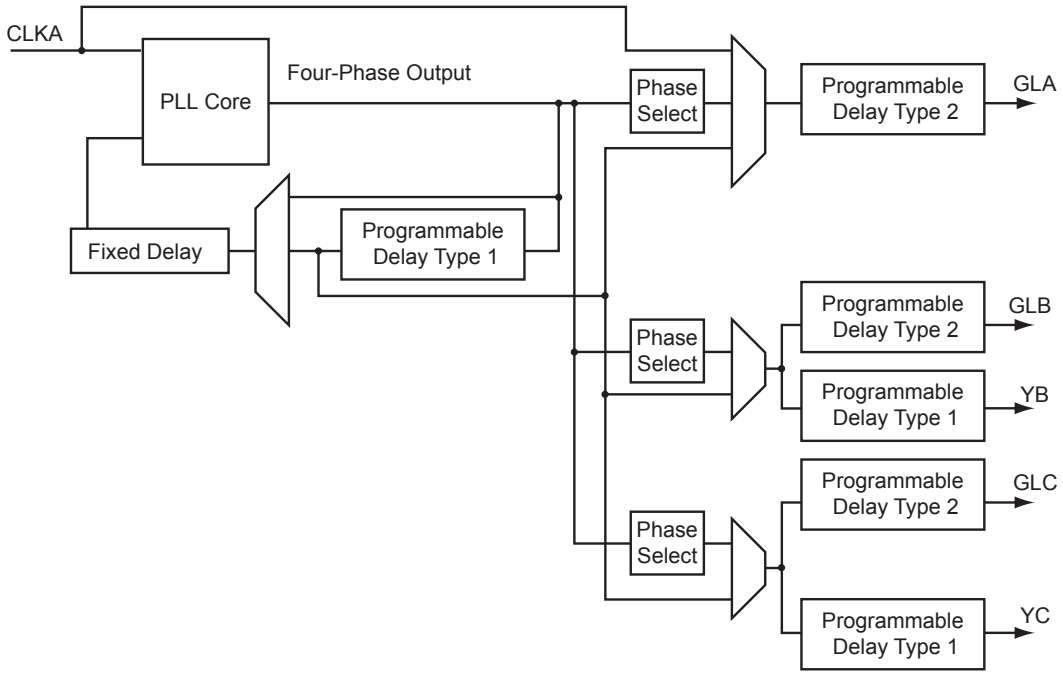
CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.

Figure 2-23 • **PLL Block**

PLL Macro

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLKA input of the CCC block, which is only accessible from the global A[2:0] package pins. Refer to Figure 2-22 on page 2-25 for more information.

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL feedback loop can be driven either internally or externally. The PLL macro also provides power-down input and lock output signals. During power-up, POWERDOWN should be asserted Low until V_{CC} is up. See Figure 2-19 on page 2-22 for more information.

Inputs:

- CLKA: selected clock input
- POWERDOWN (active low): disables PLLs. The default state is power-down on (active low).

Outputs:

- LOCK (active high): indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. Figure 2-23 on page 2-26 illustrates the various clock output options and delay elements.

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global networks, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate it from the hardwired I/O connection described earlier.

The visual PLL configuration in SmartGen, available with the Libero IDE and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. SmartGen allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select where the input clock is coming from. SmartGen automatically instantiates the special macro, PLLINT, when needed.

CCC and PLL Characteristics

Timing Characteristics

Table 2-11 • Fusion CCC/PLL Specification

Parameter		Min.	Typ.	Max.	Unit
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		350	MHz
Delay Increments in Programmable Delay Blocks[1,2]			160		ps
Number of Programmable Values in Each Programmable Delay Block				32	
Input Period Jitter				1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}		Max Peak-to-Peak Period Jitter			
		1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz		0.50%		0.70%	
24 MHz to 100 MHz		1.00%		1.20%	
100 MHz to 250 MHz		1.75%		2.00%	
250 MHz to 350 MHz		2.50%		5.60%	
Acquisition Time	LockControl = 0			300	µs
	LockControl = 1			6.0	ms
Tracking Jitter[3]	LockControl = 0			1.6	ns
	LockControl = 1			0.8	ns
Output Duty Cycle		48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1,2]		0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 [1,2]		0.025		5.56	ns
Delay Range in Block: Fixed Delay[1,2]			2.2		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 3-7 on page 3-10 for deratings.*
2. *T_J = 25°C, VCC = 1.5 V*
3. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*

No-Glitch MUX (NGMUX)

Positioned downstream from the PLL/CCC blocks, the NGMUX provides a special switching sequence between two asynchronous clock domains that prevents generating any unwanted narrow clock pulses. The NGMUX is used to switch the source of a global between three different clock sources. Allowable inputs are either two PLL/CCC outputs or a PLL/CCC output and a regular net, as shown in Figure 2-24. The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal or GLC). These are set by SmartGen during design but can also be changed by dynamically reconfiguring the PLL. The GLMUXSEL[1:0] bits control which clock source is passed through the NGMUX to the global network (GL). See Table 2-12.

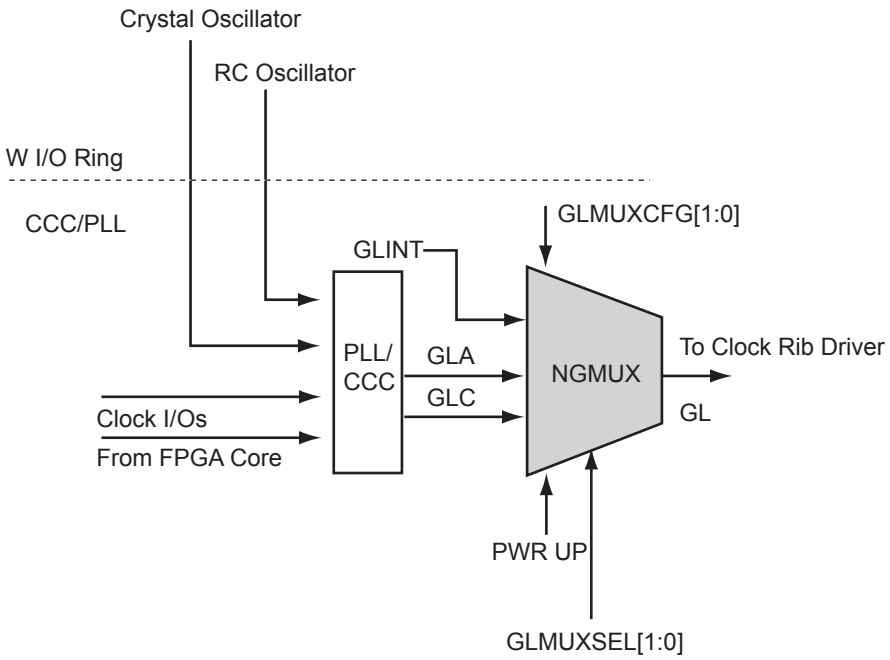


Figure 2-24 • **NGMUX**

Table 2-12 • **NGMUX Configuration and Selection Table**

GLMUXCFG[1:0]	GLMUXSEL[1:0]		Selected Input Signal	MUX Type
00	X	0	GLA	2-to-1 GLMUX
	X	1	GLC	
01	X	0	GLA	2-to-1 GLMUX
	X	1	GLINT	

The NGMUX macro is simplified to show the two clock options that have been selected by the GLMUXCFG[1:0] bits. Figure 2-25 illustrates the NGMUX macro. During design, the two clock sources are connected to CLK0 and CLK1 and are controlled by GLMUXSEL[1:0] to determine which signal is to be passed through the MUX.

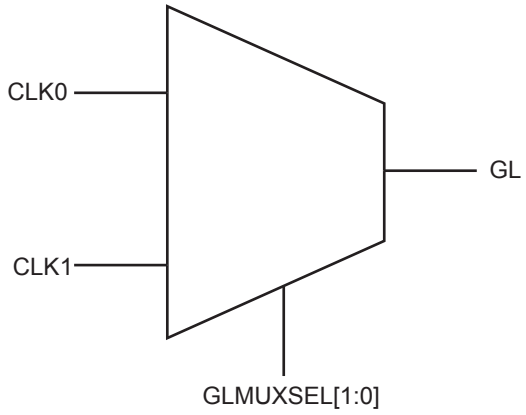


Figure 2-25 • **NGMUX Macro**

The sequence of switching between two clock sources (from CLK0 to CLK1) is as follows (Figure 2-26):

- GLMUXSEL[1:0] transitions to initiate a switch.
- GL drives one last complete CLK0 positive pulse (i.e., one rising edge followed by one falling edge).
- From that point, GL stays Low until the second rising edge of CLK1 occurs.
- At the second CLK1 rising edge, GL will begin to continuously deliver the CLK1 signal.
- Minimum t_{sw} = 0.05 ns at 25°C (typical conditions)

For examples of NGMUX operation, refer to the *Fusion FPGA Fabric User's Guide*.

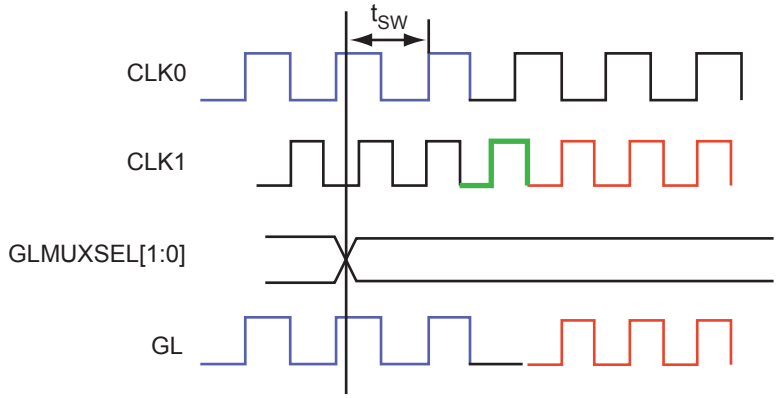


Figure 2-26 • **NGMUX Waveform**

Real-Time Counter System

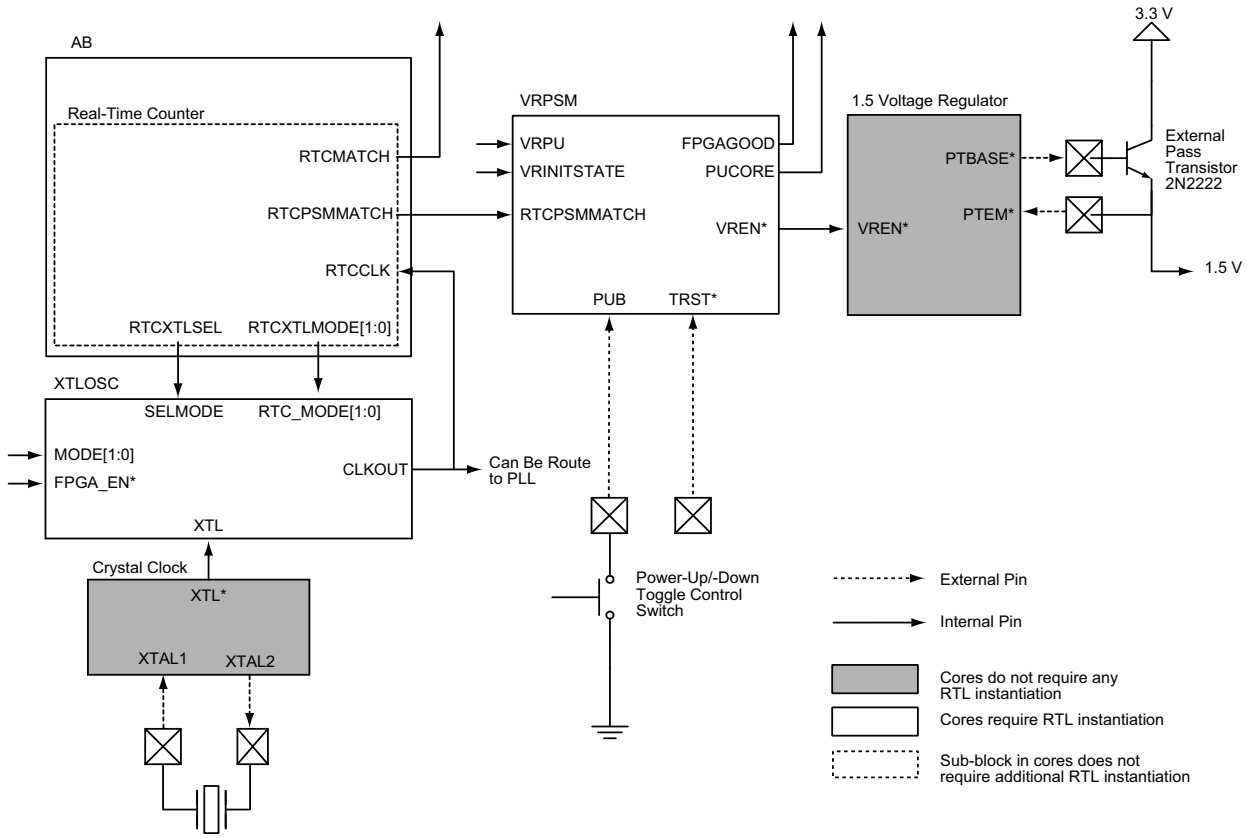
The RTC system enables Fusion devices to support standby and sleep modes of operation to reduce power consumption in many applications.

- Sleep mode, typical 10 µA
- Standby mode (RTC running), typical 3 mA with 20 MHz

The RTC system is composed of five cores:

- RTC sub-block inside Analog Block (AB)
- Voltage Regulator and Power System Monitor (VRPSM)
- Crystal oscillator (XTLOSC); refer to the "Crystal Oscillator" section in the Fusion Clock Resources chapter of the *Fusion FPGA Fabric User's Guide* for more detail.
- Crystal clock; does not require instantiation in RTL
- 1.5 V voltage regulator; does not require instantiation in RTL

All cores are powered by 3.3 V supplies, so the RTC system is operational without a 1.5 V supply during standby mode. Figure 2-27 shows their connection.



*Note: *Signals are hardwired internally and do not exist in the macro core.*

Figure 2-27 • **Real-Time Counter System (not all the signals are shown for the AB macro)**

Modes of Operation

Standby Mode

Standby mode allows periodic power-up and power-down of the FPGA fabric. In standby mode, the real-time counter and crystal block are ON. The FPGA is not powered by disabling the 1.5 V voltage regulator. The 1.5 V voltage regulator can be enabled when the preset count is matched. Refer to the "Real-Time Counter (part of AB macro)" section for details. To enter standby mode, the RTC must be first configured and enabled. Then VRPSM is shut off by deasserting the VRPU signal. The 1.5 V voltage regulator is then disabled, and shuts off the 1.5 V output.

Sleep Mode

In sleep mode, the real-time counter and crystal blocks are OFF. The 1.5 V voltage regulator inside the VRPSM can only be enabled by the PUB or TRST pin. Refer to the "Voltage Regulator and Power System Monitor (VRPSM)" section on page 2-35 for details on power-up and power-down of the 1.5 V voltage regulator.

Standby and Sleep Mode Circuit Implementation

For extra power savings, V_{JTAG} and V_{PP} should be at the same voltage as V_{CC}, floated or ground, during standby and sleep modes. Note that when V_{JTAG} is not powered, the 1.5 V voltage regulator cannot be enabled through TRST.

V_{PP} and V_{JTAG} can control through an external switch. Actel recommends ADG839, ADG849, or ADG841 as possible switches. Figure 2-28 shows the implementation for controlling V_{PP}. The IN signal of the switch can be connected to PTBASE of the Fusion device. V_{JTAG} can be controlled in same manner.

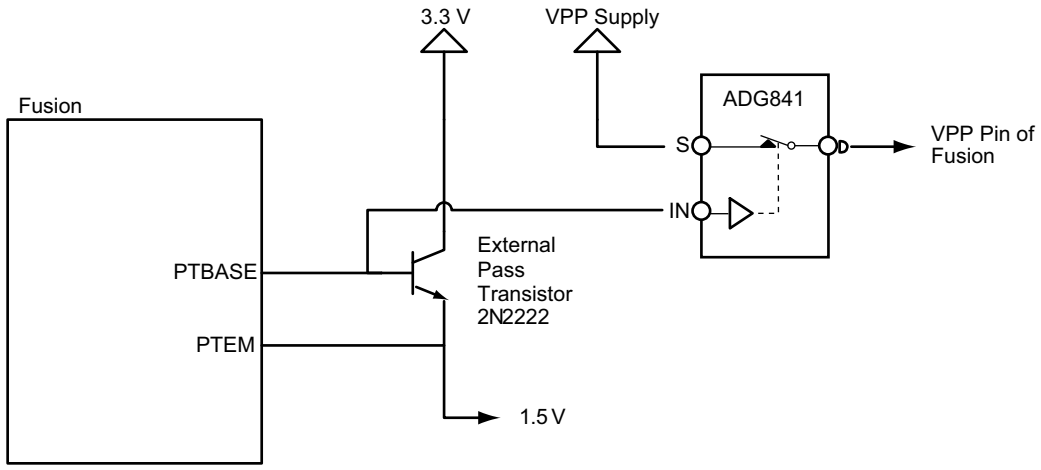


Figure 2-28 • **Implementation to Control VPP**

Real-Time Counter (part of AB macro)

The RTC is a 40-bit loadable counter and used as the primary timekeeping element (Figure 2-29). The clock source, RTCCLK, must come from the CLKOUT signal of the crystal oscillator. The RTC can be configured to reset itself when a count value reaches the match value set in the Match Register.

The RTC is part of the Analog Block (AB) macro. The RTC is configured by the analog configuration MUX (ACM). Each address contains one byte of data. The circuitry in the RTC is powered by V_{CC33A}, so the RTC can be used in standby mode when the 1.5 V supply is not present.

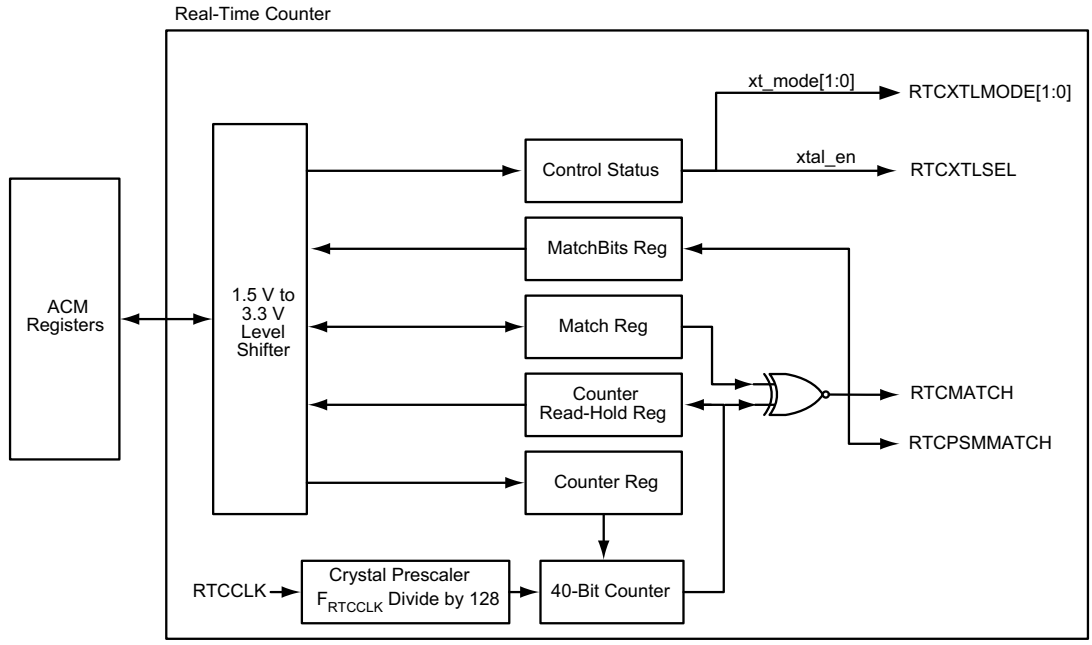


Figure 2-29 • **RTC Block Diagram**

Table 2-13 • **RTC Signal Description**

Signal Name	Width	Direction	Function
RTCCLK	1	In	Must come from CLKOUT of XTLOSC.
RTCXTLMODE[1:0]	2	Out	Controlled by xt_mode in CTRL_STAT. Signal must connect to the RTC_MODE signal in XTLOSC, as shown in Figure 2-27.
RTCXTLSEL	1	Out	Controlled by xtal_en from CTRL_STAT register. Signal must connect to RTC_MODE signal in XTLOSC in Figure 2-27.
RTCMATCH	1	Out	Match signal for FPGA 0 – Counter value does not equal the Match Register value. 1 – Counter value equals the Match Register value.
RTCPSMMATCH	1	Out	Same signal as RTCMATCH. Signal must connect to RTCPSMMATCH in VRPSM, as shown in Figure 2-27.

The 40-bit counter can be preloaded with an initial value as a starting point by the Counter Register. The count from the 40-bit counter can be read through the same set of address space. The count comes from a Read-Hold Register to avoid data changing during read.

When the counter value equals the Match Register value, all Match Bits Register values will be 0xFFFFFFFFFF. The RTCMATCH and RTCPSMMATCH signals will assert. The 40-bit counter can be configured to automatically reset to 0x0000000000 when the counter value equals the Match Register value. The automatic reset does not apply if the Match Register value is 0x0000000000.

The RTCCLK has a prescaler to divide the clock by 128 before it is used for the 40-bit counter. Below is an example of how to calculate the OFF time.

Example: Calculation for Match Count

To put the Fusion device on standby for one hour using an external crystal of 32.768 KHz:

The period of the crystal oscillator is $T_{crystal}$:

$T_{crystal}$ = 1 / 32.768 KHz = 30.518 µs

The period of the counter is $T_{counter}$:

$T_{counter}$ = 30.518 us X 128 = 3.90625 ms

The Match Count for 1 hour is ∆tmatch:

∆tmatch / $T_{counter}$ = (1 hr X 60 min/hr X 60 sec/min) / 3.90625 ms = 921600 or 0xE1000

Using a 32.768 KHz crystal, the maximum standby time of the 40-bit counter is 4,294,967,296 seconds, which is 136 years.

Table 2-14 • **Memory Map for RTC in ACM Register and Description**

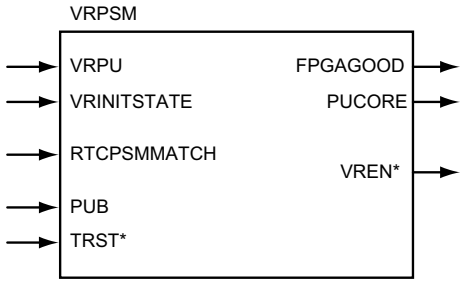
ACMADDR	Register Name	Description	Use	Default Value
0x40	COUNTER0	Counter bits 7:0	Used to preload the counter to a specified start point.	0x00
0x41	COUNTER1	Counter bits 15:8		0x00
0x42	COUNTER2	Counter bits 23:16		0x00
0x43	COUNTER3	Counter bits 31:24		0x00
0x44	COUNTER4	Counter bits 39:32		0x00
0x48	MATCHREG0	Match register bits 7:0	The RTC comparison bits	0x00
0x49	MATCHREG1	Match register bits 15:8		0x00
0x4A	MATCHREG2	Match register bits 23:16		0x00
0x4B	MATCHREG3	Match register bits 31:24		0x00
0x4C	MATCHREG4	Match register bits 39:32		0x00
0x50	MATCHBIT0	Individual match bits 7:0	The output of the XNOR gates 0 – Not matched 1 – Matched	0x00
0x51	MATCHBIT1	Individual match bits 15:8		0x00
0x52	MATCHBIT2	Individual match bits 23:16		0x00
0x53	MATCHBIT3	Individual match bits 31:24		0x00
0x54	MATCHBIT4	Individual match bits 29:32		0x00
0x58	CTRL_STAT	Control (write/read) / Status (read only) register bits	Refer to Table 2-15 on page 2-35 for details.	0x00

Table 2-15 • **RTC Control/Status Register**

Bit	Name	Description	Default Value
7	rtc_rst	RTC Reset 1 – Resets the RTC 0 – Deassert reset on after two ACM_CLK cycle.	
6	cntr_en	Counter Enable 1 – Enables the counter; rtc_rst must be deasserted as well. First counter increments after 64 RTCCLK positive edges. 0 – Disables the crystal prescaler but does not reset the counter value. Counter value can only be updated when the counter is disabled.	0
5	vr_en_mat	Voltage Regulator Enable on Match 1 – Enables RTCMATCH and RTCPSMMATCH to output 1 when the counter value equals the Match Register value. This enables the 1.5 V voltage regulator when RTCPSMMATCH connects to the RTCPSMMATCH signal in VRPSM. 0 – RTCMATCH and RTCPSMMATCH output 0 at all times.	0
4:3	xt_mode[1:0]	Crystal Mode Controls RTCXTLMODE[1:0]. Connects to RTC_MODE signal in XTLOSC. XTL_MODE uses this value when xtal_en is 1. See the "Crystal Oscillator" section on page 2-18 for mode configuration.	00
2	rst_cnt_omat	Reset Counter on Match 1 – Enables the sync clear of the counter when the counter value equals the Match Register value. The counter clears on the rising edge of the clock. If all the Match Registers are set to 0, the clear is disabled. 0 – Counter increments indefinitely	0
1	rstb_cnt	Counter Reset, active Low 0 – Resets the 40-bit counter value	0
0	xtal_en	Crystal Enable Controls RTCXTLSEL. Connects to SELMODE signal in XTLOSC. 0 – XTLOSC enables control by FPGA_EN; xt_mode is not used. Sleep mode requires this bit to equal 0. 1 – Enables XTLOSC, XTL_MODE control by xt_mode Standby mode requires this bit to be set to 1. See the "Crystal Oscillator" section on page 2-18 for further details on SELMODE configuration.	0

Voltage Regulator and Power System Monitor (VRPSM)

The VRPSM macro controls the power-up state of the FPGA. The power-up bar (PUB) pin can turn on the voltage regulator when set to 0. TRST can enable the voltage regulator when deasserted, allowing the FPGA to power-up when user want access to JTAG ports. The inputs VRINITSTATE and RTCPSMMATCH come from the flash bits and RTC, and can also power up the FPGA



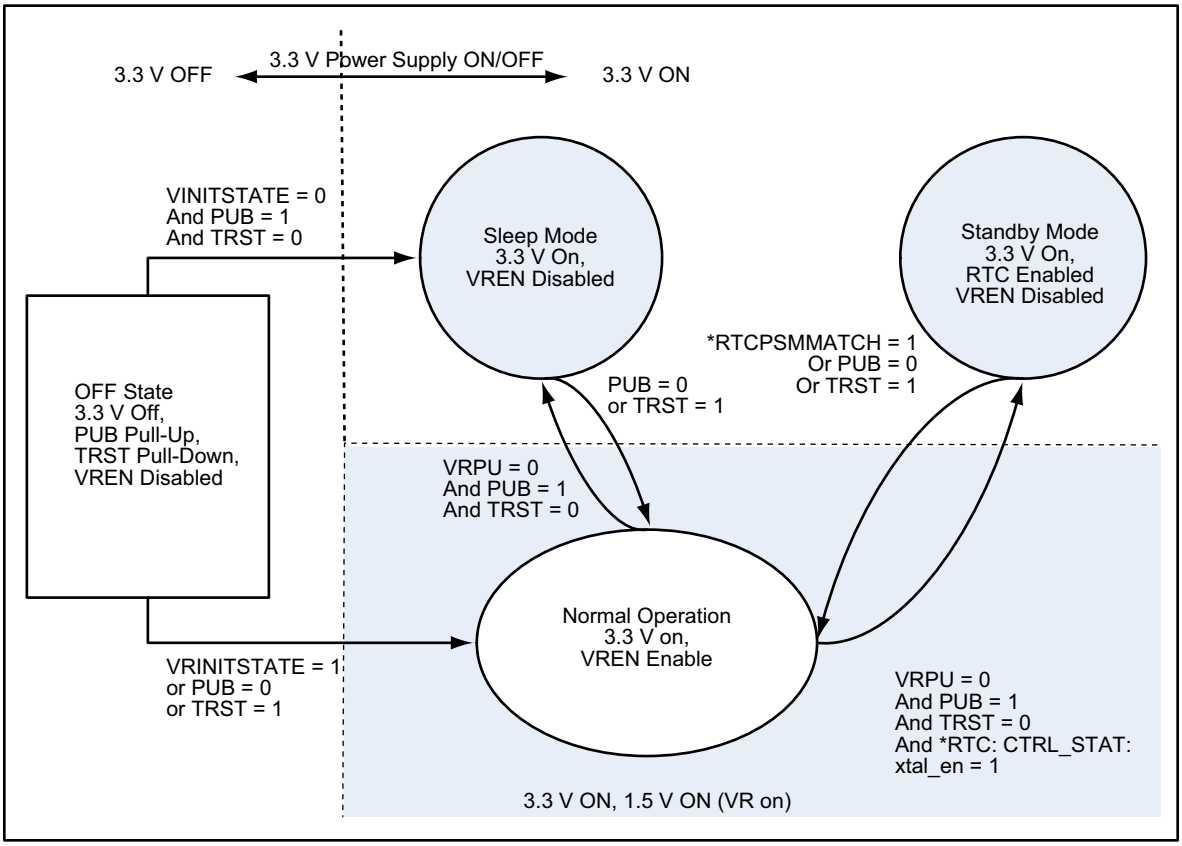
*Note: *Signals are hardwired internally and do not exist in the macro core.*

Figure 2-30 • **VRPSM Macro**

Table 2-16 • **VRPSM Signal Descriptions**

Signal Name	Width	Dir.	Function
VRPU	1	In	Voltage Regulator Power-Up 0 – Voltage regulator disabled. PUB must be floated or pulled up, and the TRST pin must be grounded to disable the voltage regulator. 1 – Voltage regulator enabled
VRINITSTATE	1	In	Voltage Regulator Initial State Defines the voltage regulator status upon power-up of the 3.3 V. The signal is configured by Actel Libero IDE when the VRPSM macro is generated. Tie off to 1 – Voltage regulator enables when 3.3 V is powered. Tie off to 0 – Voltage regulator disables when 3.3 V is powered.
RTCPSMMATCH	1	In	RTC Power System Management Match Connect from RTCPSMATCH signal from RTC in AB 0 transition to 1 turns on the voltage regulator
PUB	1	In	External pin, built-in weak pull-up Power-Up bar 0 – Enables voltage regulator at all times
TRST*	1	In	External pin, JTAG Test Reset 1 – Enables voltage regulator at all times
FPGAGOOD	1	Out	Indicator that the FPGA is powered and functional No need to connect if it is not used. 1 – Indicates that the FPGA is powered up and functional. 0 – Not possible to read by FPGA since it has already powered off.
PUCORE	1	Out	Power-Up Core Inverted signal of PUB. No need to connect if it is not used.
VREN*	1	Out	Voltage Regulator Enable Connected to 1.5 V voltage regulator in Fusion device internally. 0 – Voltage regulator disables 1 – Voltage regulator enables

*Note: *Signals are hardwired internally and do not exist in the macro core.*



*Note: *To enter and exit standby mode without any external stimulus on PUB or TRST, the vr_en_mat in the CTRL_STAT register must also be set to 1, so that RTCPSMMATCH will assert when a match occurs; hence the device exits standby mode.*

Figure 2-31 • **State Diagram for All Different Power Modes**

When TRST is 1 or PUB is 0, the 1.5 V voltage regulator is always ON, putting the Fusion device in normal operation at all times. Therefore, when the JTAG port is not in reset, the Fusion device cannot enter sleep mode or standby mode.

To enter standby mode, the Fusion device must first power-up into normal operation. The RTC is enabled through the RTC Control/Status Register described in the "Real-Time Counter (part of AB macro)" section on page 2-33. A match value corresponding to the wake-up time is loaded into the Match Register. The 1.5 V voltage regulator is disabled by setting VRPU to 0 to allow the Fusion device to enter standby mode, when the 1.5 V supply is off but the RTC remains on.

1.5 V Voltage Regulator

The 1.5 V voltage regulator uses an external pass transistor to generate 1.5 V from a 3.3 V supply. The base of the pass transistor is tied to PTBASE, the collector is tied to 3.3 V, and an emitter is tied to PTBASE and the 1.5 V supplies of the Fusion device. Figure 2-27 on page 2-31 shows the hook-up of the 1.5 V voltage regulator to an external pass transistor.

Actel recommends using a PN2222A or 2N2222A transistor. The gain of such a transistor is approximately 25, with a maximum base current of 20 mA. The maximum current that can be supported is 0.5 A. Transistors with different gain can also be used for different current requirements.

Table 2-17 • **Electrical Characteristics**
VCC33A = 3.3 V

Symbol	Parameter	Condition		Min	Typical	Max	Units
V_{OUT}	Output Voltage	T_J = 25ºC		1.425	1.5	1.575	V
I_{CC33A}	Operation Current	T_J = 25ºC	I_{LOAD} = 1 mA I_{LOAD} = 100 mA I_{LOAD} = 0.5 A		11 11 30		mA mA mA
Δ_{VOUT}	Load Regulation	T_J = 25ºC	I_{LOAD} = 1 mA to 0.5 A		90		mV
Δ_{VOUT}	Line Regulation	T_J = 25ºC	VCC33A = 2.97 V to 3.63 V I_{LOAD} = 1 mA VCC33A = 2.97 V to 3.63 V I_{LOAD} = 100 mA VCC33A = 2.97 V to 3.63 V I_{LOAD} = 500 mA		 10.6 12.1 10.6		 mV/V mV/V mV/V
	Dropout Voltage*	T_J = 25ºC	I_{LOAD} = 1 mA I_{LOAD} = 100 mA I_{LOAD} = 0.5 A		0.63 0.84 1.35		V V V
I_{PTBASE}	PTBase Current	T_J = 25ºC	I_{LOAD} = 1 mA I_{LOAD} = 100 mA I_{LOAD} = 0.5 A		48 736 12	 20	µA µA mA

*Note: *Data collected with 2N2222A.*

Embedded Memories

Fusion devices include four types of embedded memory: flash block, FlashROM, SRAM, and FIFO.

Flash Memory Block

Fusion is the first FPGA that offers a flash memory block (FB). Each FB block stores 2 Mbits of data. The flash memory block macro is illustrated in Figure 2-32. The port pin name and descriptions are detailed on Table 2-18 on page 2-40. All flash memory block signals are active high, except for CLK and active low RESET. All flash memory operations are synchronous to the rising edge of CLK.

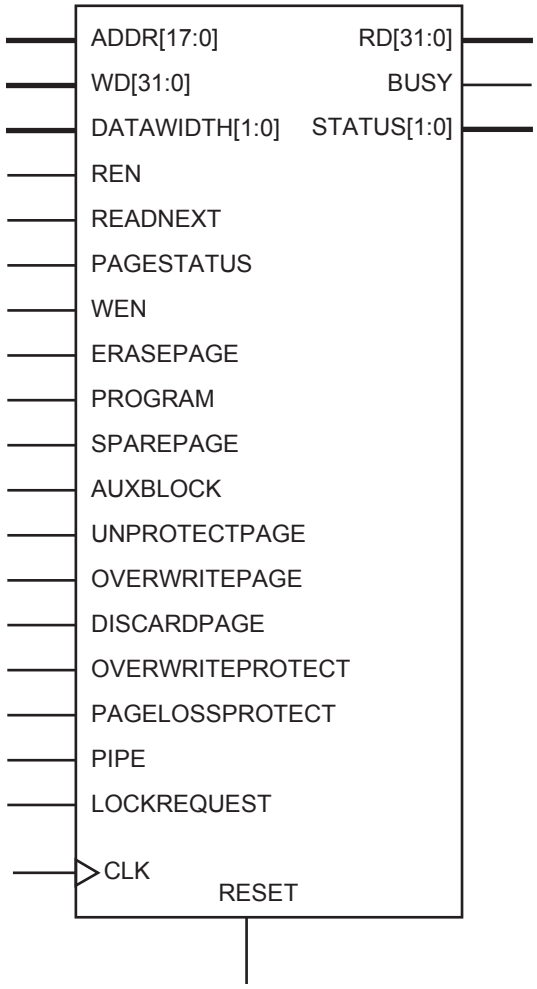


Figure 2-32 • **Flash Memory Block**

Flash Memory Block Pin Names

Table 2-18 • Flash Memory Block Pin Names

Interface Name	Width	Direction	Description
ADDR[17:0]	18	In	Byte offset into the FB. Byte-based address.
AUXBLOCK	1	In	When asserted, the page addressed is used to access the auxiliary block within that page.
BUSY	1	Out	When asserted, indicates that the FB is performing an operation.
CLK	1	In	User interface clock. All operations and status are synchronous to the rising edge of this clock.
DATAWIDTH[1:0]	2	In	Data width 00 = 1 byte in RD/WD[7:0] 01 = 2 bytes in RD/WD[15:0] 1x = 4 bytes in RD/WD[31:0]
DISCARDPAGE	1	In	When asserted, the contents of the Page Buffer are discarded so that a new page write can be started.
ERASEPAGE	1	In	When asserted, the address page is to be programmed with all zeros. ERASEPAGE must transition synchronously with the rising edge of CLK.
LOCKREQUEST	1	In	When asserted, indicates to the JTAG controller that the FPGA interface is accessing the FB.
OVERWRITEPAGE	1	In	When asserted, the page addressed is overwritten with the contents of the Page Buffer if the page is writable.
OVERWRITEPROTECT	1	In	When asserted, all program operations will set the overwrite protect bit of the page being programmed.
PAGESTATUS	1	In	When asserted with REN, initiates a read page status operation.
PAGELOSSPROTECT	1	In	When asserted, a modified Page Buffer must be programmed or discarded before accessing a new page.
PIPE	1	In	Adds a pipeline stage to the output for operation above 50 MHz.
PROGRAM	1	In	When asserted, writes the contents of the Page Buffer into the FB page addressed.
RD[31:0]	32	Out	Read data; data will be valid from the first non-busy cycle (BUSY = 0) after REN has been asserted.
READNEXT	1	In	When asserted with REN, initiates a read-next operation.
REN	1	In	When asserted, initiates a read operation.
RESET	1	In	When asserted, resets the state of the FB (active low).
SPAREPAGE	1	In	When asserted, the sector addressed is used to access the spare page within that sector.

Table 2-18 • **Flash Memory Block Pin Names (continued)**

Interface Name	Width	Direction	Description
STATUS[1:0]	2	Out	Status of the last operation completed: 00: Successful completion 01: Read-/Unprotect-Page: single error detected and corrected Write: operation addressed a write-protected page Erase-Page: protection violation Program: Page Buffer is unmodified Protection violation 10: Read-/Unprotect-Page: two or more errors detected 11: Write: attempt to write to another page before programming current page Erase-Page/Program: page write count has exceeded the 10-year retention threshold
UNPROTECTPAGE	1	In	When asserted, the page addressed is copied into the Page Buffer and the Page Buffer is made writable.
WD[31:0]	32	In	Write data
WEN	1	In	When asserted, stores WD in the page buffer.

All flash memory block input signals are active high, except for RESET.

Flash Memory Block Diagram

A simplified diagram of the flash memory block is shown in Figure 2-33.

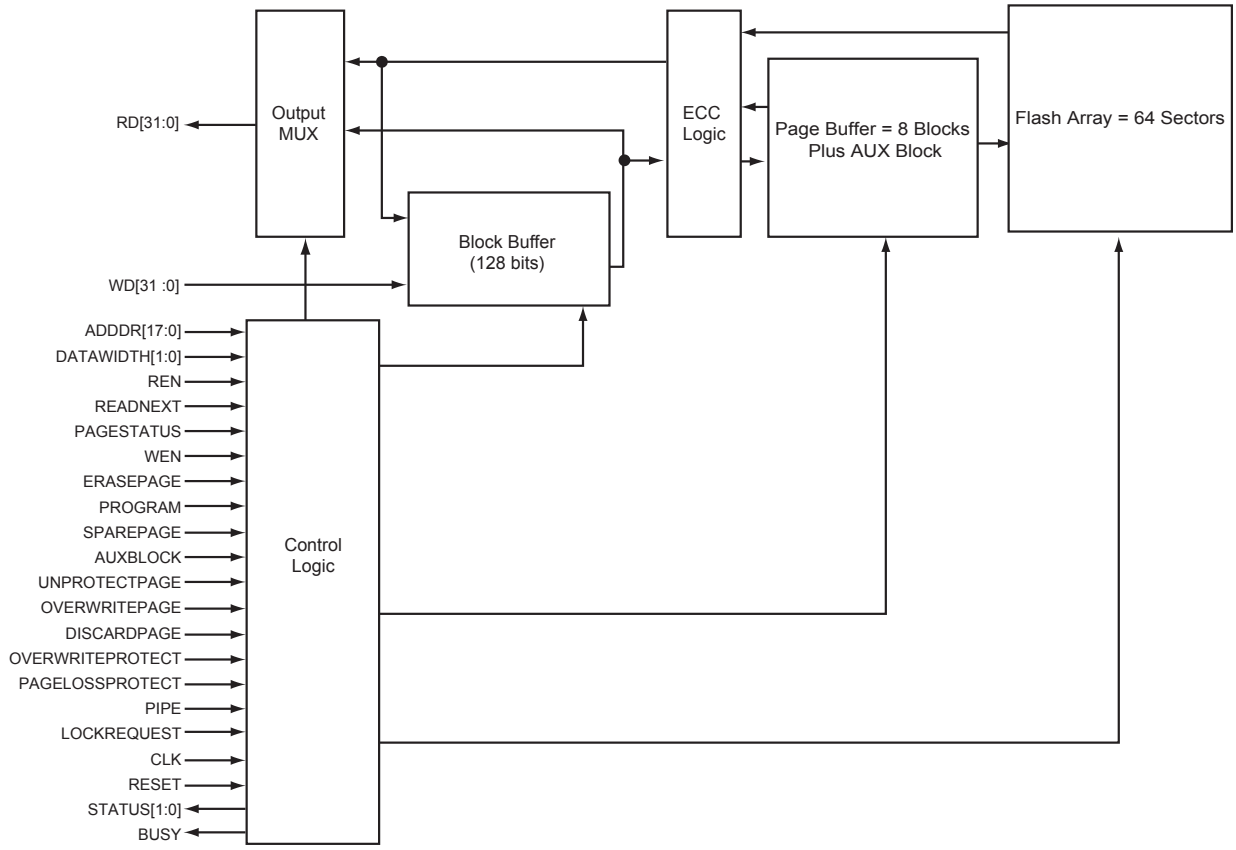


Figure 2-33 • **Flash Memory Block Diagram**

The logic consists of the following sub-blocks:

- Flash Array

  Contains all stored data. The flash array contains 64 sectors, and each sector contains 33 pages of data.
- Page Buffer

  A page-wide volatile register. A page contains 8 blocks of data and an AUX block.
- Block Buffer

  Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic

The FB stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

Flash Memory Block Addressing

Figure 2-34 shows a graphical representation of the flash memory block.

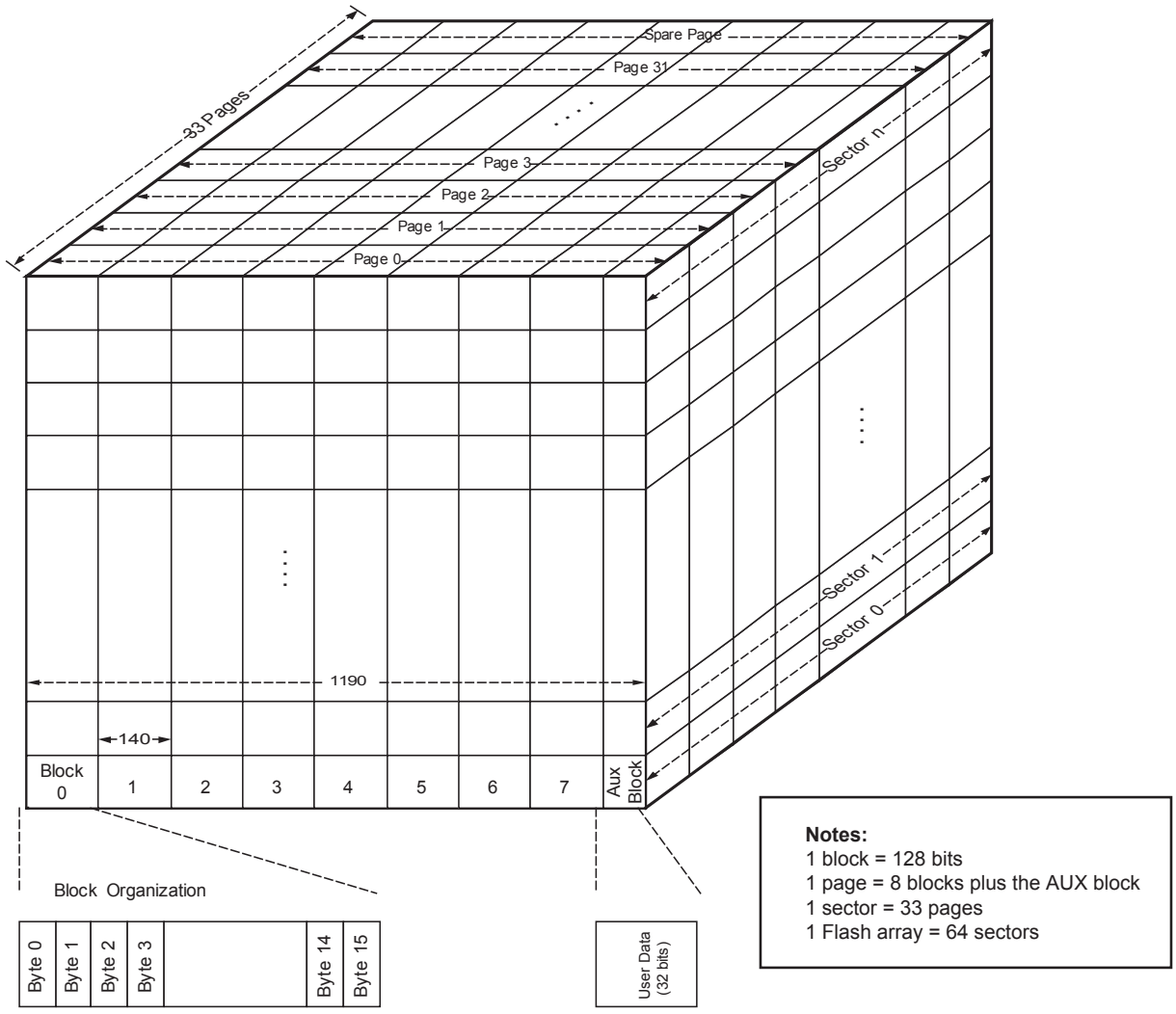


Figure 2-34 • **Flash Memory Block Organization**

Each FB is partitioned into sectors, pages, blocks, and bytes. There are 64 sectors in an FB, and each sector contains 32 pages and 1 spare page. Each page contains 8 data blocks and 1 auxiliary block. Each data block contains 16 bytes of user data, and the auxiliary block contains 4 bytes of user data.

Addressing for the FB is shown in Table 2-19.

Table 2-19 • **FB Address Bit Allocation ADDR[17:0]**

17	12	11	7	6	4	3	0
Sector		Page		Block		Byte	

When the spare page of a sector is addressed (SPAREPAGE active), ADDR[11:7] are ignored.

When the Auxiliary block is addressed (AUXBLOCK active), ADDR[6:2] are ignored.

Note: The spare page of sector 0 is unavailable for any user data. Writes to this page will return an error, and reads will return all zeroes.

Data operations are performed in widths of 1 to 4 bytes. A write to a location in a page that is not already in the Page Buffer will cause the page to be read from the FB Array and stored in the Page Buffer. The block that was addressed during the write will be put into the Block Buffer, and the data written by WD will overwrite the data in the Block Buffer. After the data is written to the Block Buffer, the Block Buffer is then written to the Page Buffer to keep both buffers in sync. Subsequent writes to the same block will overwrite the Block Buffer and the Page Buffer. A write to another block in the page will cause the addressed block to be loaded from the Page Buffer, and the write will be performed as described previously.

The data width can be selected dynamically via the DATAWIDTH input bus. The truth table for the data width settings is detailed in Table 2-20. The minimum resolvable address is one 8-bit byte. For data widths greater than 8 bits, the corresponding address bits are ignored—when DATAWIDTH = 0 (2 bytes), ADDR[0] is ignored, and when DATAWIDTH = '10' or '11' (4 bytes), ADDR[1:0] are ignored. Data pins are LSB-oriented and unused WD data pins must be grounded.

Table 2-20 • **Data Width Settings**

DATAWIDTH[1:0]	Data Width
00	1 byte [7:0]
01	2 byte [15:0]
10, 11	4 bytes [31:0]

Flash Memory Block Protection

Page Loss Protection

When the PAGELOSSPROTECT pin is set to logic 1, it prevents writes to any page other than the current page in the Page Buffer until the page is either discarded or programmed.

A write to another page while the current page is Page Loss Protected will return a STATUS of '11'.

Overwrite Protection

Any page that is Overwrite Protected will result in the STATUS being set to '01' when an attempt is made to either write, program, or erase it. To set the Overwrite Protection state for a page, set the OVERWRITEPROTECT pin when a Program operation is undertaken. To clear the Overwrite Protect state for a given page, an Unprotect Page operation must be performed on the page, and then the page must be programmed with the OVERWRITEPROTECT pin cleared to save the new page.

LOCKREQUEST

The LOCKREQUEST signal is used to give the user interface control over simultaneous access of the FB from both the User and JTAG interfaces. When LOCKREQUEST is asserted, the JTAG interface will hold off any access attempts until LOCKREQUEST is deasserted.

Flash Memory Block Operations

FB Operation Priority

The FB provides for priority of operations when multiple actions are requested simultaneously. Table 2-21 shows the priority order (priority 0 is the highest).

Table 2-21 • **FB Operation Priority**

Operation	Priority
System Initialization	0
FB Reset	1
Read	2
Write	3
Erase Page	4
Program	5
Unprotect Page	6
Discard Page	7

Access to the FB is controlled by the BUSY signal. The BUSY output is synchronous to the CLK signal. FB operations are only accepted in cycles where BUSY is logic 0.

Write Operation

Write operations are initiated with the assertion of the WEN signal. Figure 2-35 illustrates the multiple Write operations.

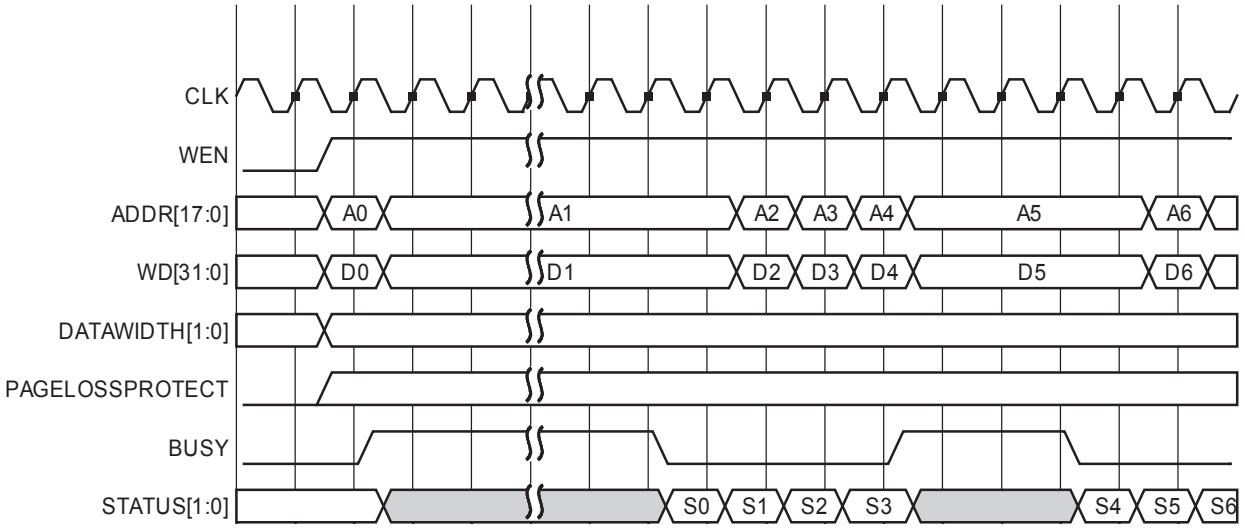


Figure 2-35 • **FB Write Waveform**

When a Write operation is initiated to a page that is currently not in the Page Buffer, the FB control logic will issue a BUSY signal to the user interface while the page is loaded from the FB Array into the Page Buffer. (Note: The number of clock cycles that the BUSY output is asserted during the load of the Page Buffer is variable.) After loading the page into the Page Buffer, the addressed data block is loaded from the Page Buffer into the Block Buffer. Subsequent writes to the same block of the page will incur no busy cycles. A write to another block in the page will assert BUSY for four cycles (five cycles when PIPE is asserted), to allow the data to be written to the Page Buffer and have the current block loaded into the Block Buffer.

Write operations are considered successful as long as the STATUS output is '00'. A non-zero STATUS indicates that an error was detected during the operation and the write was not performed. Note that the STATUS output is "sticky"; it is unchanged until another operation is started.

Only one word can be written at a time. Write word width is controlled by the DATAWIDTH bus. Users are responsible for keeping track of the contents of the Page Buffer and when to program it to the array. Just like a regular RAM, writing to random addresses is possible. Users can write into the Page Buffer in any order but will incur additional BUSY cycles. It is not necessary to modify the entire Page Buffer before saving it to nonvolatile memory.

Write errors include the following:

1. Attempting to write a page that is Overwrite Protected (STATUS = '01'). The write is not performed.
2. Attempting to write to a page that is not in the Page Buffer when Page Loss Protection is enabled (STATUS = '11'). The write is not performed.

Program Operation

A Program operation is initiated by asserting the PROGRAM signal on the interface. Program operations save the contents of the Page Buffer to the FB Array. Due to the technologies inherent in the FB, a program operation is a time consuming operation (~8 ms). While the FB is writing the data to the array, the BUSY signal will be asserted.

During a Program operation, the sector and page addresses on ADDR are compared with the stored address for the page (and sector) in the Page Buffer. If there is a mismatch between the two addresses, the Program operation will be aborted and an error will be reported on the STATUS output.

It is possible to write the Page Buffer to a different page in memory. When asserting the PROGRAM pin, if OVERWRITEPAGE is asserted as well, the FB will write the contents of the Page Buffer to the sector and page designated on the ADDR inputs if the destination page is not Overwrite Protected.

A Program operation can be utilized to either modify the contents of the page in the flash memory block or change the protections for the page. Setting the OVERWRITEPROTECT bit on the interface while asserting the PROGRAM pin will put the page addressed into Overwrite Protect Mode. Overwrite Protect Mode safeguards a page from being inadvertently overwritten during subsequent Program or Erase operations.

Program operations that result in a STATUS value of '01' do not modify the addressed page. For all other values of STATUS, the addressed page is modified.

Program errors include the following:

1. Attempting to program a page that is Overwrite Protected (STATUS = '01')
2. Attempting to program a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection Mode (STATUS = '01')
3. Attempting to perform a program with OVERWRITEPAGE set when the page addressed has been Overwrite Protected (STATUS = '01')
4. The Write Count of the page programmed exceeding the Write Threshold defined in the part specification (STATUS = '11')
5. The ECC Logic determining that there is an uncorrectable error within the programmed page (STATUS = '10')
6. Attempting to program a page that is **not** in the Page Buffer when OVERWRITEPAGE is not set and the page in the Page Buffer is modified (STATUS = '01')
7. Attempting to program the page in the Page Buffer when the Page Buffer is **not** modified

The waveform for a Program operation is shown in Figure 2-36.

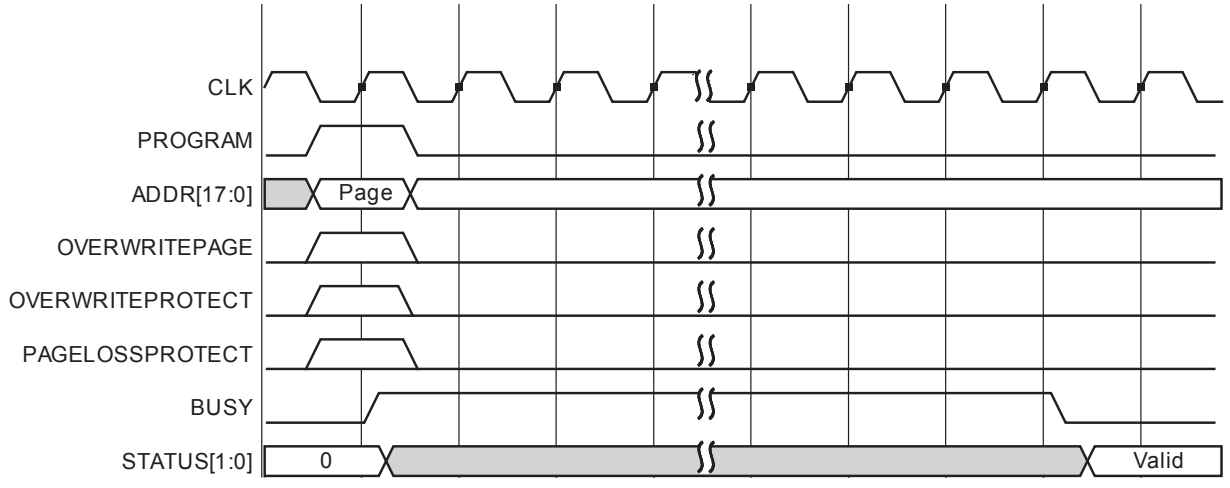


Figure 2-36 • **FB Program Waveform**

Note: OVERWRITEPAGE is only sampled when the PROGRAM or ERASEPAGE pins are asserted. OVERWRITEPAGE is ignored in all other operations.

Erase Page Operation

The Erase Page operation is initiated when the ERASEPAGE pin is asserted. The Erase Page operation allows the user to erase (set user data to zero) any page within the FB.

The use of the OVERWRITEPAGE and PAGELOSSPROTECT pins is the same for erase as for a Program Page operation.

As with the Program Page operation, a STATUS of '01' indicates that the addressed page is not erased.

A waveform for an Erase Page operation is shown in Figure 2-37.

Erase errors include the following:

1. Attempting to erase a page that is Overwrite Protected (STATUS = '01')
2. Attempting to erase a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection mode (STATUS = '01')
3. The Write Count of the erased page exceeding the Write Threshold defined in the part specification (STATUS = '11')
4. The ECC Logic determining that there is an uncorrectable error within the erased page (STATUS = '10')

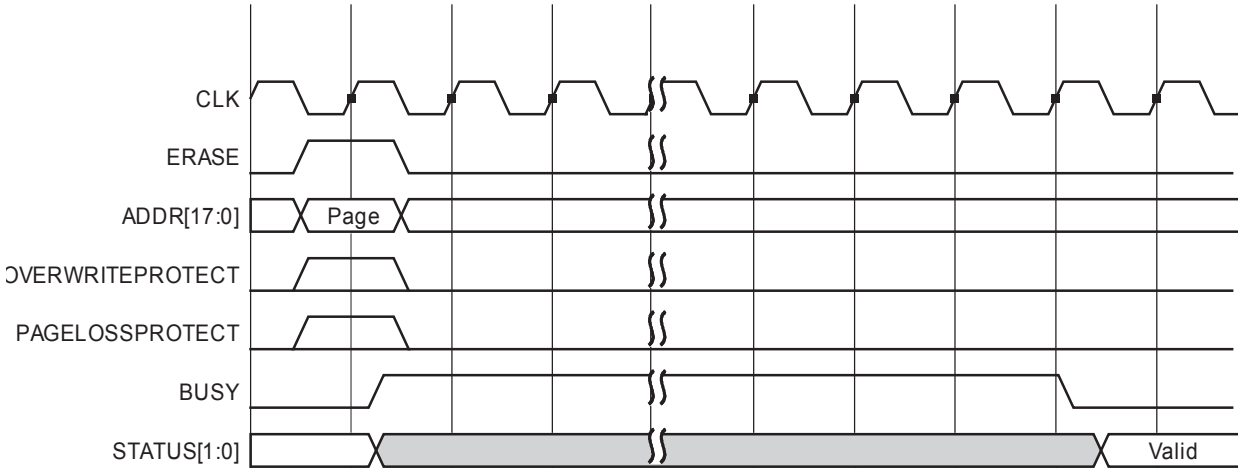


Figure 2-37 • **FB Erase Page Waveform**

Read Operation

Read operations are designed to read data from the FB Array, Page Buffer, Block Buffer, or status registers. Read operations support a normal read and a read-ahead mode (done by asserting READNEXT). Also, the timing for Read operations is dependent on the setting of PIPE.

The following diagrams illustrate representative timing for Non-Pipe Mode (Figure 2-38) and Pipe Mode (Figure 2-39) reads of the flash memory block interface.

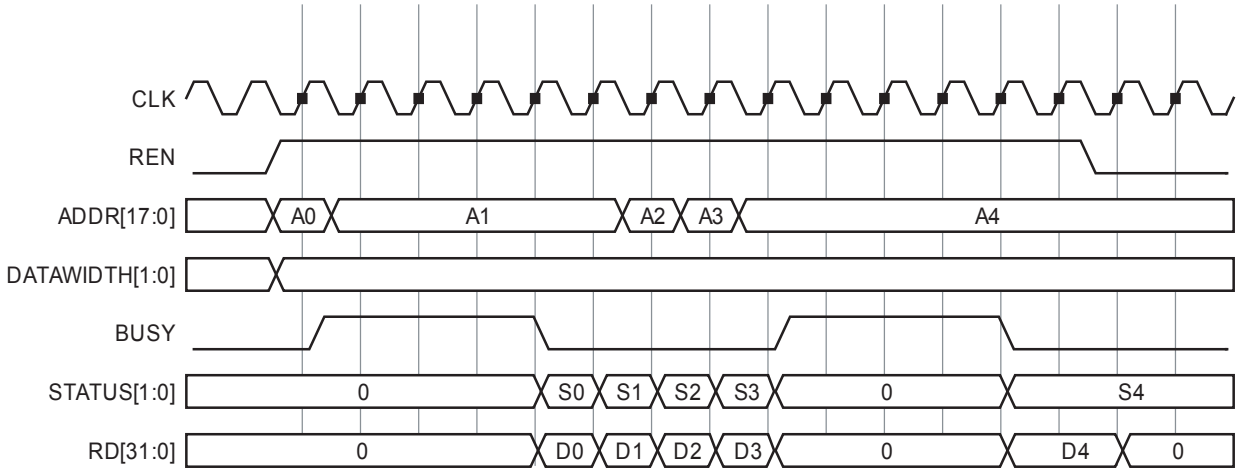


Figure 2-38 • **Read Waveform (Non-Pipe Mode, 32-bit access)**

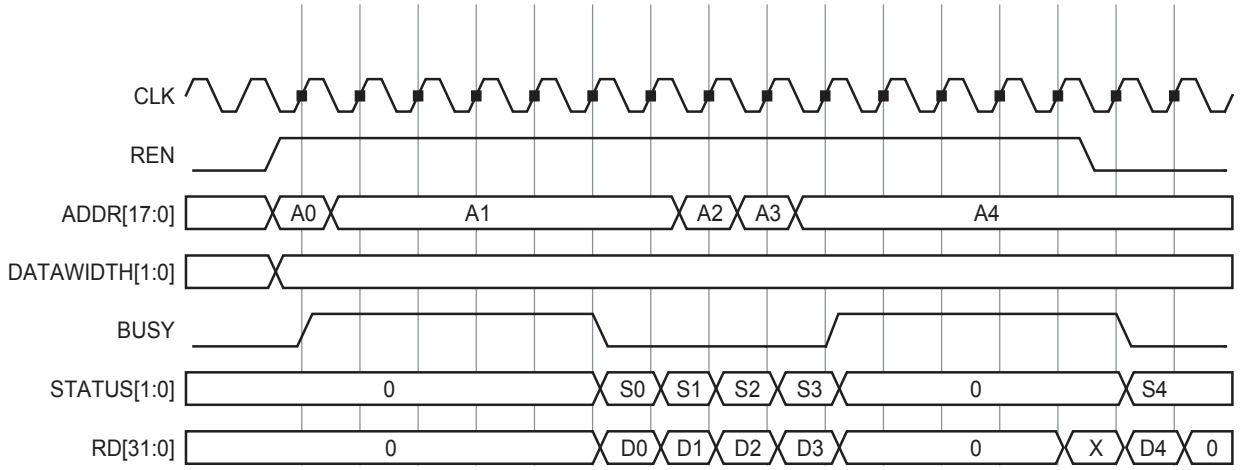


Figure 2-39 • **Read Waveform (Pipe Mode, 32-bit access)**

The following error indications are possible for Read operations:

1. STATUS = '01' when a single-bit data error was detected and corrected within the block addressed.
2. STATUS = '10' when a double-bit error was detected in the block addressed (note that the error is uncorrected).

In addition to data reads, users can read the status of any page in the FB by asserting PAGESTATUS along with REN. The format of the data returned by a page status read is shown in Table 2-22, and the definition of the page status bits is shown in Table 2-23.

Table 2-22 • **Page Status Read Data Format**

31	8	7	4	3	2	1	0
Write Count		Reserved		Over Threshold	Read Protected	Write Protected	Overwrite Protected

Table 2-23 • **Page Status Bit Definition**

Page Status Bit(s)	Definition
31–8	The number of times the page addressed has been programmed/erased
7–4	Reserved; read as 0
3	Over Threshold indicator (see the "Program Operation" section on page 2-46)
2	Read Protected; read protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
1	Write Protected; write protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
0	Overwrite Protected; designates that the user has set the OVERWRITEPROTECT bit on the interface while doing a Program operation. The page cannot be written without first performing an Unprotect Page operation.

Read Next Operation

The Read Next operation is a feature by which the next block relative to the block in the Block Buffer is read from the FB Array while performing reads from the Block Buffer. The goal is to minimize wait states during consecutive sequential Read operations.

The Read Next operation is performed in a predetermined manner because it does look-ahead reads. The general look-ahead function is as follows:

- Within a page, the next block fetched will be the next in linear address.
- When reading the last data block of a page, it will fetch the first block of the next page.
- When reading spare pages, it will read the first block of the next sector's spare page.
- Reads of the last sector will wrap around to sector 0.
- Reads of Auxiliary blocks will read the next linear page's Auxiliary block.

When an address on the ADDR input does not agree with the predetermined look-ahead address, there is a time penalty for this access. The FB will be busy finishing the current look-ahead read before it can start the next read. The worst case is a total of nine BUSY cycles before data is delivered.

The Non-Pipe Mode and Pipe Mode waveforms for Read Next operations are illustrated in Figure 2-40 and Figure 2-41.

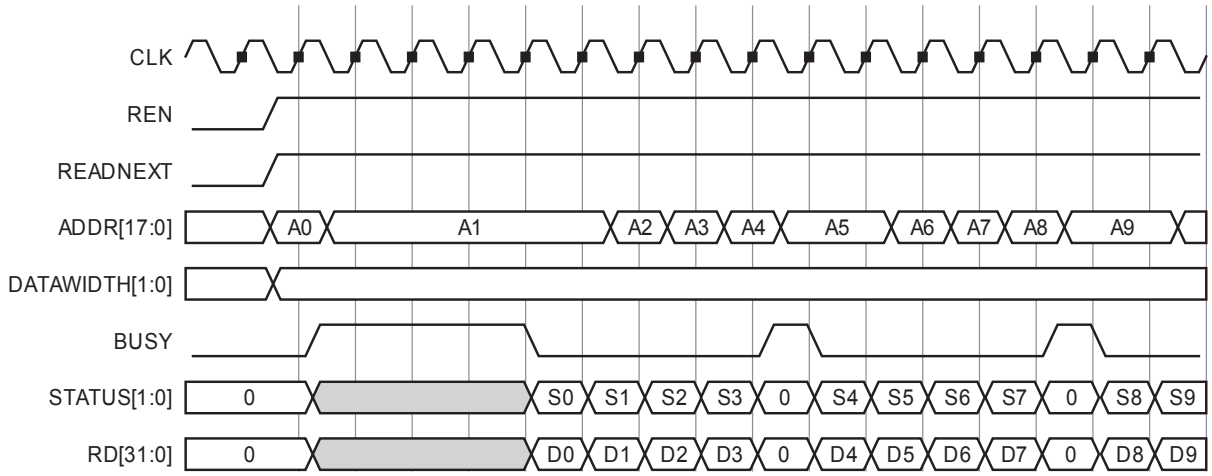


Figure 2-40 • **Read Next Waveform (Non-Pipe Mode, 32-bit access)**

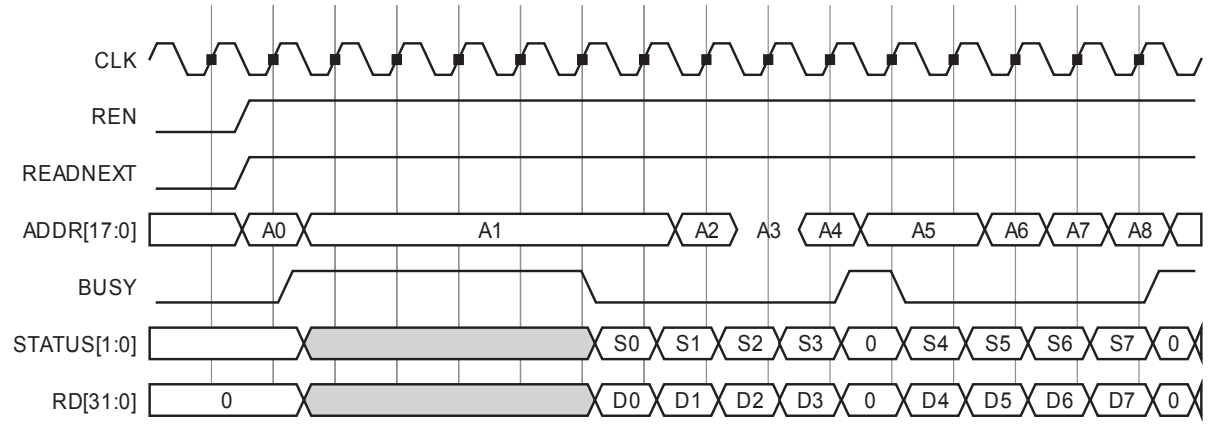


Figure 2-41 • **Read Next WaveForm (Pipe Mode, 32-bit access)**

Unprotect Page Operation

An Unprotect Page operation will clear the protection for a page addressed on the ADDR input. It is initiated by setting the UNPROTECTPAGE signal on the interface along with the page address on ADDR.

If the page is not in the Page Buffer, the Unprotect Page operation will copy the page into the Page Buffer. The Copy Page operation occurs only if the current page in the Page Buffer is not Page Loss Protected.

The waveform for an Unprotect Page operation is shown in Figure 2-42.

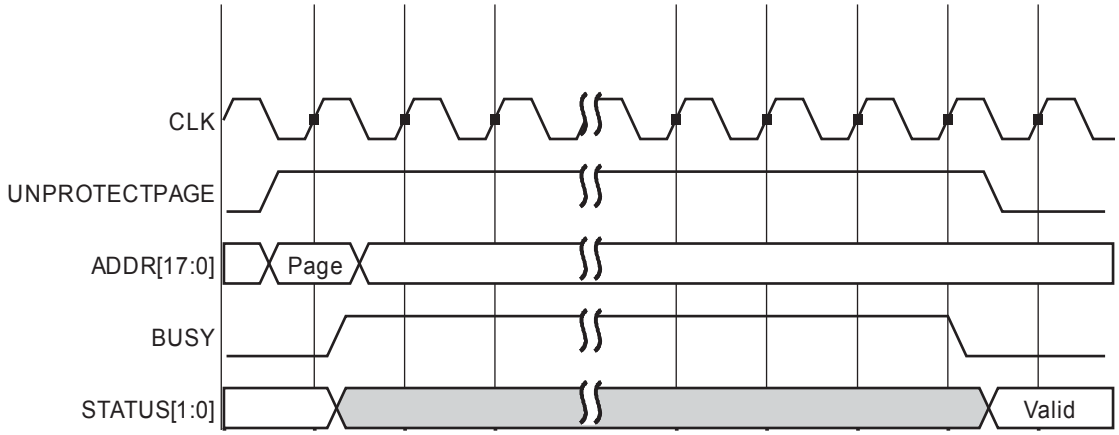


Figure 2-42 • **FB Unprotected Page Waveform**

The Unprotect Page operation can incur the following error conditions:

1. If the copy of the page to the Page Buffer determines that the page has a single-bit correctable error in the data, it will report a STATUS = '01'.
2. If the address on ADDR does not match the address of the Page Buffer, PAGELOSSPROTECT is asserted, and the Page Buffer has been modified, then STATUS = '11' and the addressed page is not loaded into the Page Buffer.
3. If the copy of the page to the Page Buffer determines that at least one block in the page has a double-bit uncorrectable error, STATUS = '10' and the Page Buffer will contain the corrupted data.

Discard Page Operation

If the contents of the modified Page Buffer have to be discarded, the DISCARDPAGE signal should be asserted. This command results in the Page Buffer being marked as unmodified.

The timing for the operation is shown in Figure 2-43. The BUSY signal will remain asserted until the operation has completed.

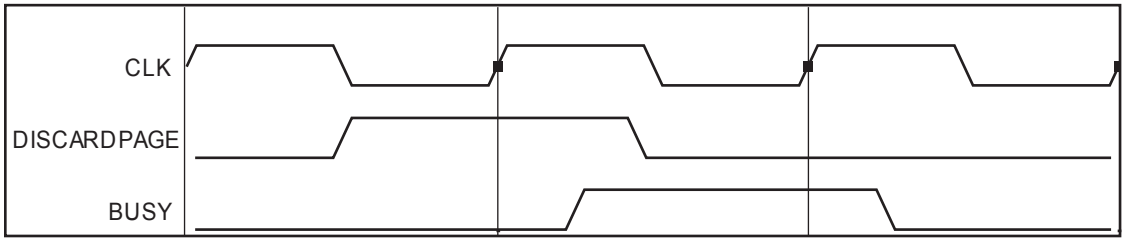


Figure 2-43 • **FB Discard Page Waveform**

Flash Memory Block Characteristics

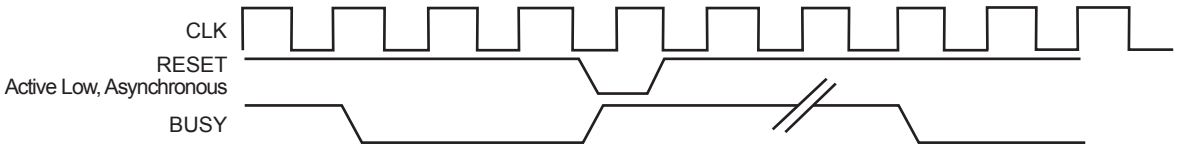


Figure 2-44 • **Reset Timing Diagram**

Table 2-24 • **Flash Memory Block Timing, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V**

Parameter	Description	–2	–1	Std.	Units
t_{CLK2RD}	Clock-to-Q in 5-cycle read mode of the Read Data	8.24	9.39	11.04	ns
	Clock-to-Q in 6-cycle read mode of the Read Data	5.10	5.81	6.83	ns
$t_{CLK2BUSY}$	Clock-to-Q in 5-cycle read mode of BUSY	5.19	5.91	6.95	ns
	Clock-to-Q in 6-cycle read mode of BUSY	4.59	5.23	6.15	ns
$t_{CLK2STATUS}$	Clock-to-Status in 5-cycle read mode	11.59	13.21	15.53	ns
	Clock-to-Status in 6-cycle read mode	4.62	5.26	6.19	ns
t_{DSUNVM}	Data Input Setup time for the Control Logic	1.98	2.26	2.65	ns
t_{DHNVM}	Data Input Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{ASUNVM}	Address Input Setup time for the Control Logic	2.84	3.24	3.81	ns
t_{AHNVM}	Address Input Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUDWNVM}$	Data Width Setup time for the Control Logic	1.91	2.17	2.56	ns
$t_{HDDWNVM}$	Data Width Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SURENNVM}$	Read Enable Setup time for the Control Logic	3.97	4.53	5.32	ns
$t_{HDRENNVM}$	Read Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUWENNVM}$	Write Enable Setup time for the Control Logic	2.44	2.78	3.27	ns
$t_{HDWENNVM}$	Write Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUPROGNVM}$	Program Setup time for the Control Logic	2.23	2.54	2.98	ns
$t_{HDPROGNVM}$	Program Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUSPAREPAGE}$	SparePage Setup time for the Control Logic	3.86	4.40	5.17	ns
$t_{HDSPAREPAGE}$	SparePage Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUAUXBLK}$	Auxiliary Block Setup Time for the Control Logic	3.85	4.39	5.16	ns
$t_{HDAUXBLK}$	Auxiliary Block Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SURDNEXT}$	ReadNext Setup Time for the Control Logic	2.23	2.54	2.99	ns
$t_{HDRDNEXT}$	ReadNext Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUERASEPG}$	Erase Page Setup Time for the Control Logic	3.87	4.41	5.19	ns
$t_{HDERASEPG}$	Erase Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUUNPROTECTPG}$	Unprotect Page Setup Time for the Control Logic	2.07	2.36	2.77	ns
$t_{HDUNPROTECTPG}$	Unprotect Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUDISCARDPG}$	Discard Page Setup Time for the Control Logic	1.94	2.21	2.60	ns
$t_{HDDISCARDPG}$	Discard Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUOVERWRPRO}$	Overwrite Protect Setup Time for the Control Logic	1.69	1.92	2.26	ns
$t_{HDOVERWRPRO}$	Overwrite Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns

Table 2-24 • Flash Memory Block Timing, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V (continued)

Parameter	Description	–2	–1	Std.	Units
$t_{SUPGLOSSPRO}$	Page Loss Protect Setup Time for the Control Logic	1.74	1.99	2.34	ns
$t_{HDPGLOSSPRO}$	Page Loss Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUPGSTAT}$	Page Status Setup Time for the Control Logic	2.56	2.92	3.43	ns
$t_{HDPGSTAT}$	Page Status Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUOVERWRPG}$	Over Write Page Setup Time for the Control Logic	1.94	2.21	2.60	ns
$t_{HDOVERWRPG}$	Over Write Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SULOCKREQUEST}$	Lock Request Setup Time for the Control Logic	0.90	1.02	1.20	ns
$t_{HDLOCKREQUEST}$	Lock Request Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{RECARNVM}$	Reset Recovery Time	0.97	1.10	1.29	ns
$t_{REMARNVM}$	Reset Removal Time	0.00	0.00	0.00	ns
$t_{MPWARNVM}$	Asynchronous Reset Minimum Pulse Width for the Control Logic	12.50	15.63	15.63	ns
$t_{MPWCLKNVM}$	Clock Minimum Pulse Width for the Control Logic	5.00	6.25	6.25	ns
$t_{FMAXCLKNVM}$	Maximum Frequency for Clock for the Control Logic	80.00	64.00	64.00	MHz

FlashROM

Fusion devices have 1 kbit of on-chip nonvolatile flash memory that can be read from the FPGA core fabric. The FlashROM is arranged in eight banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read-back of the FlashROM from the FPGA core (Figure 2-45).

The FlashROM can only be programmed via the IEEE 1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the eight 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports a synchronous read and can be read on byte boundaries. The upper three bits of the FlashROM address from the FPGA core define the bank that is being accessed. The lower four bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

The maximum FlashROM access clock is 20 MHz. Figure 2-46 on page 2-55 shows the timing behavior of the FlashROM access cycle—the address has to be set up on the rising edge of the clock for DOUT to be valid on the next falling edge of the clock.

If the address is unchanged for two cycles:

- D0 becomes invalid 10 ns after the second rising edge of the clock.
- D0 becomes valid again 10 ns after the second falling edge.

If the address unchanged for three cycles:

- D0 becomes invalid 10 ns after the second rising edge of the clock.
- D0 becomes valid again 10 ns after the second falling edge.
- D0 becomes invalid 10 ns after the third rising edge of the clock.
- D0 becomes valid again 10 ns after the third falling edge.

		Byte Number in Bank 4 LSB of ADDR (READ)															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bank Number 3 MSB of ADDR (READ)	7																
	6																
	5																
	4																
	3																
	2																
	1																
	0																

Figure 2-45 • **FlashROM Architecture**

FlashROM Characteristics

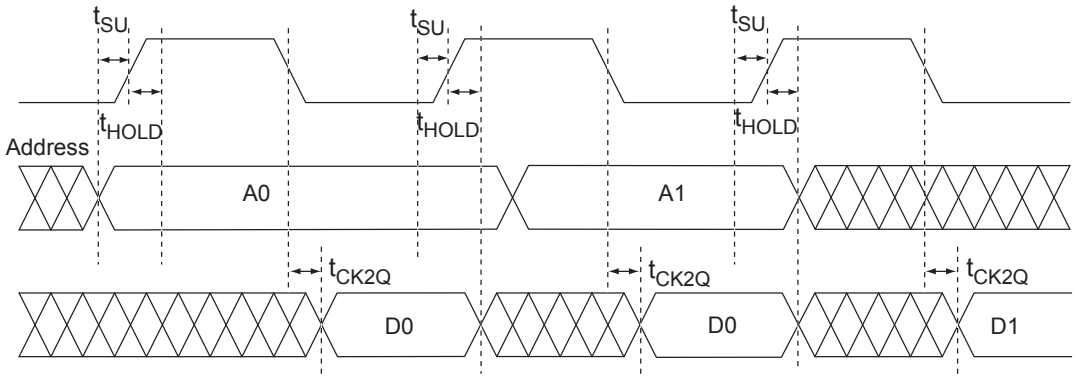


Figure 2-46 • **FlashROM Timing Diagram**

Table 2-25 • **FlashROM Access Time, Extended Temperature Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V**

Parameter	Description	–2	–1	Std.	Units
t_{SU}	Address Setup Time	0.55	0.63	0.74	ns
t_{HOLD}	Address Hold Time	0.00	0.00	0.00	ns
t_{CK2Q}	Clock to Out	16.73	19.06	22.41	ns
FMAX	Maximum Clock frequency	40.00	40.00	40.00	MHz

SRAM and FIFO

All Fusion devices have SRAM blocks along the north side of the device. Additionally, AFS600 and AFS1500 devices have an SRAM block on the south side of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz. The following configurations are available:

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—two read, two write or one read, one write)
- 512×9, 256×18 (two-port RAM—one read and one write)
- Sync write, sync pipelined/nonpipelined read

The Fusion SRAM memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

During RAM operation, addresses are sourced by the user logic, and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to Figure 2-47 for more information about the implementation of the embedded FIFO controller.

The Fusion architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. This is done with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1. For example, the write size can be set to 256×18 and the read size to 512×9.

Both the write and read widths for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in Table 2-26 on page 2-58.

When a width of one, two, or four is selected, the ninth bit is unused. For example, when writing 9-bit values and reading 4-bit values, only the first four bits and the second four bits of each 9-bit value are addressable for read operations. The ninth bit is not accessible.

Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

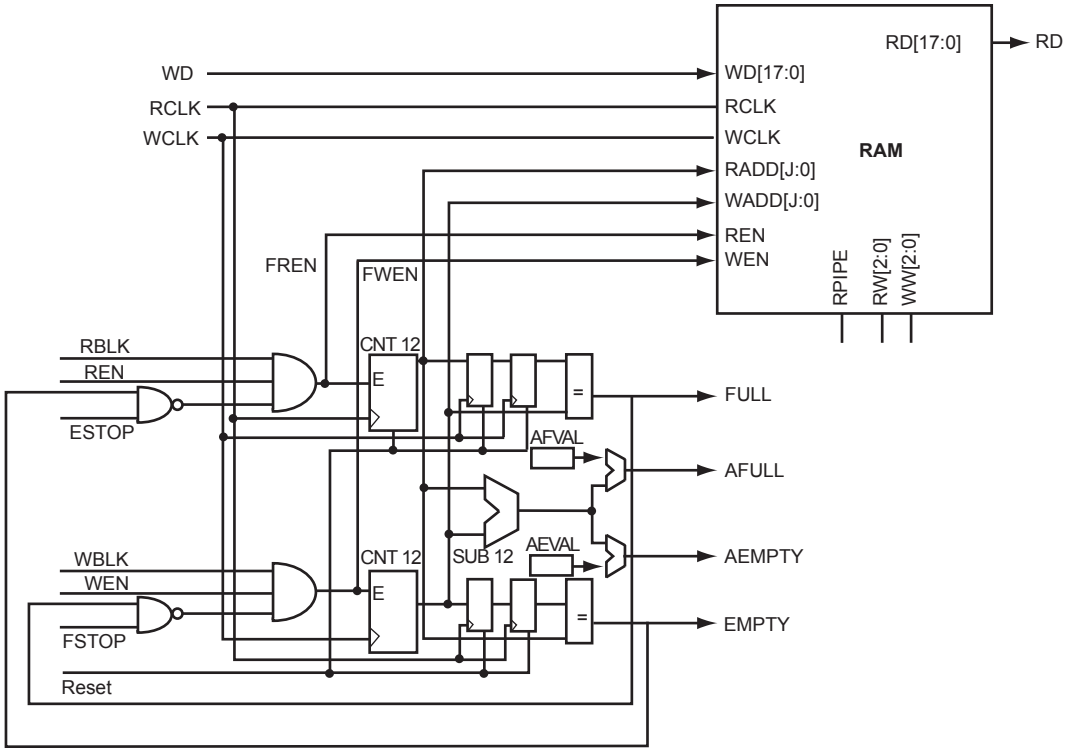


Figure 2-47 • **Fusion RAM Block with Embedded FIFO Controller**

RAM4K9 Description

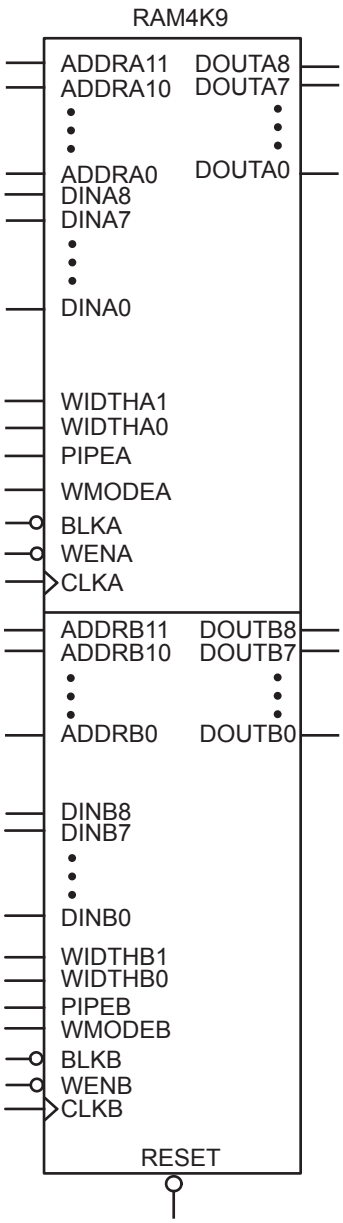


Figure 2-48 • **RAM4K9**

The following signals are used to configure the RAM4K9 memory element:

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-26).

Table 2-26 • Allowable Aspect Ratio Settings for WIDTHA[1:0]

WIDTHA1, WIDTHA0	WIDTHB1, WIDTHB0	D×W
00	00	4k×1
01	01	2k×2
10	10	1k×4
11	11	512×9

Note: The aspect ratio settings are constant and cannot be changed on the fly.

BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, the corresponding port's outputs hold the previous value.

WENA and WENB

These signals switch the RAM between read and write mode for the respective ports. A Low on these signals indicates a write operation, and a High indicates a read.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A Low on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A High indicates a pipelined, read and data appears on the corresponding output in the next clock cycle.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when the RAM is in write mode. A Low on these signals makes the output retain data from the previous read. A High indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

RESET

This active low signal resets the output to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

ADDRA and ADDRB

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-27).

Table 2-27 • Address Pins Unused/Used for Various Supported Bus Widths

	ADDRx	
D×W	Unused	Used
4k×1	None	[11:0]
2k×2	[11]	[10:0]
1k×4	[11:10]	[9:0]
512×9	[11:9]	[8:0]

Note: The "x" in ADDRx implies A or B.

DINA and DINB

These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 2-28).

DOUTA and DOUTB

These are the nine-bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used (Table 2-28). The output data on unused pins is undefined.

Table 2-28 • Unused/Used Input and Output Data Pins for Various Supported Bus Widths

D×W	DINx/DOUTx	
	Unused	Used
4k×1	[8:1]	[0]
2k×2	[8:2]	[1:0]
1k×4	[8:4]	[3:0]
512×9	None	[8:0]

Note: The "x" in DINx and DOUTx implies A or B.

RAM512X18 Description

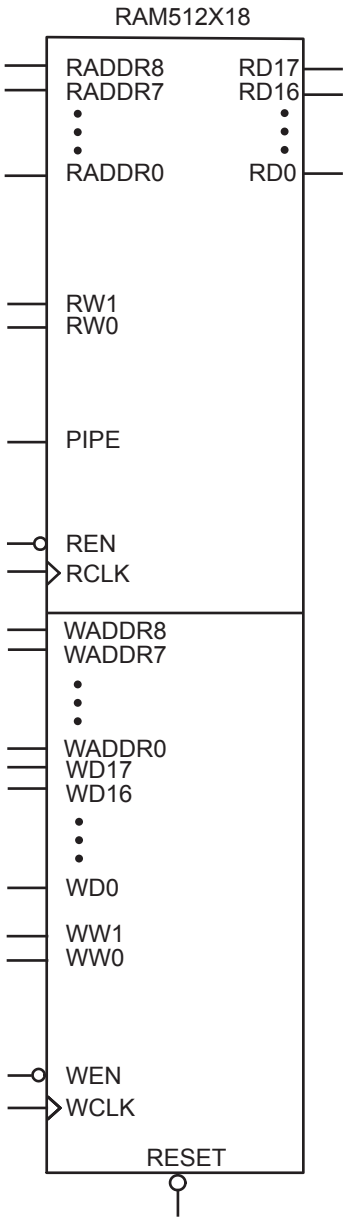


Figure 2-49 • **RAM512X18**

RAM512X18 exhibits slightly different behavior from RAM4K9, as it has dedicated read and write ports.

WW and RW

These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 2-29).

Table 2-29 • **Aspect Ratio Settings for WW[1:0]**

WW[1:0]	RW[1:0]	D×W
01	01	512×9
10	10	256×18
00, 11	00, 11	Reserved

WD and RD

These are the input and output data signals, and they are 18 bits wide. When a 512×9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, then RD[17:9] are undefined.

WADDR and RADDR

These are read and write addresses, and they are nine bits wide. When the 256×18 aspect ratio is used for write or read, WADDR[8] or RADDR[8] are unused and must be grounded.

WCLK and RCLK

These signals are the write and read clocks, respectively. They are both active high.

WEN and REN

These signals are the write and read enables, respectively. They are both active low by default. These signals can be configured as active high.

RESET

This active low signal resets the output to zero, disables reads and/or writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

PIPE

This signal is used to specify pipelined read on the output. A Low on PIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

Clocking

The dual-port SRAM blocks are only clocked on the rising edge. SmartGen allows falling-edge-triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge or by separate clocks, by port.

Fusion devices support inversion (bubble pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising edge or falling edge of WCLK and RCLK.

If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble pushing) is automatically used within the Fusion development tools, without performance penalty.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—1 clock edge): In the standard read mode, new data is driven onto the RD bus in the same clock cycle following RA and REN valid. The read address is registered on the read port clock active edge, and data appears at RD after the RAM access time. Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—2 clock edges): The pipelined mode incurs an additional clock delay from the address to the data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.
- Write (synchronous—1 clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is High. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "SRAM Characteristics" section on page 2-63 and the "FIFO Characteristics" section on page 2-72.

RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG IEEE 1532" section on page 2-224 and the *Fusion SRAM/FIFO Blocks* application note). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

SRAM Characteristics

Timing Waveforms

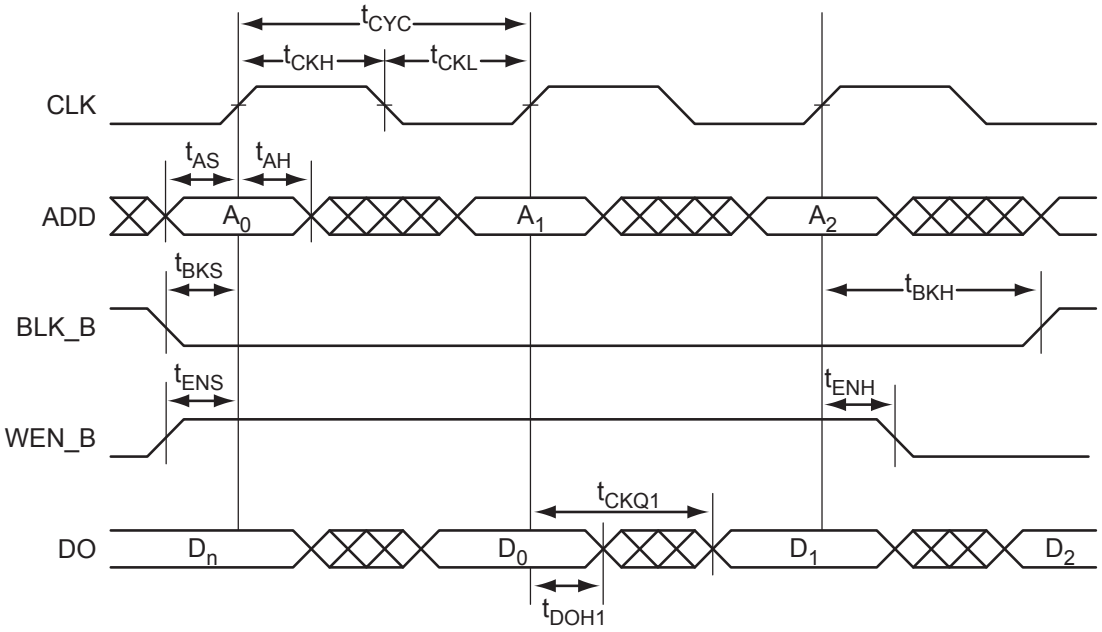


Figure 2-50 • **RAM Read for Flow-Through Output**

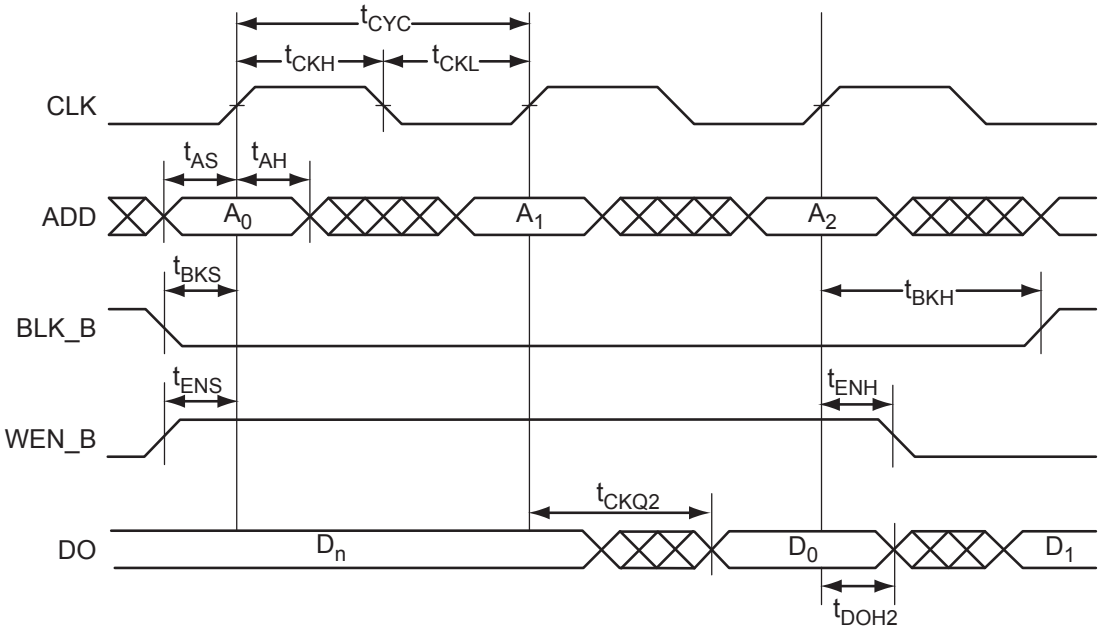


Figure 2-51 • **RAM Read for Pipelined Output**

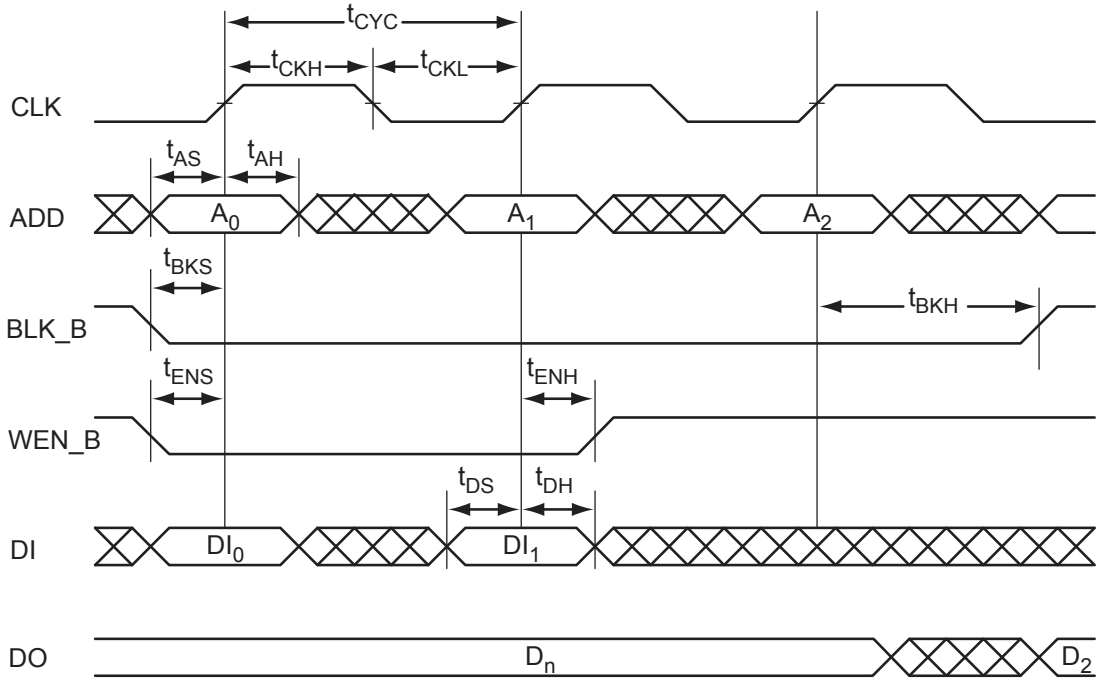


Figure 2-52 • **RAM Write, Output Retained (WMODE = 0)**

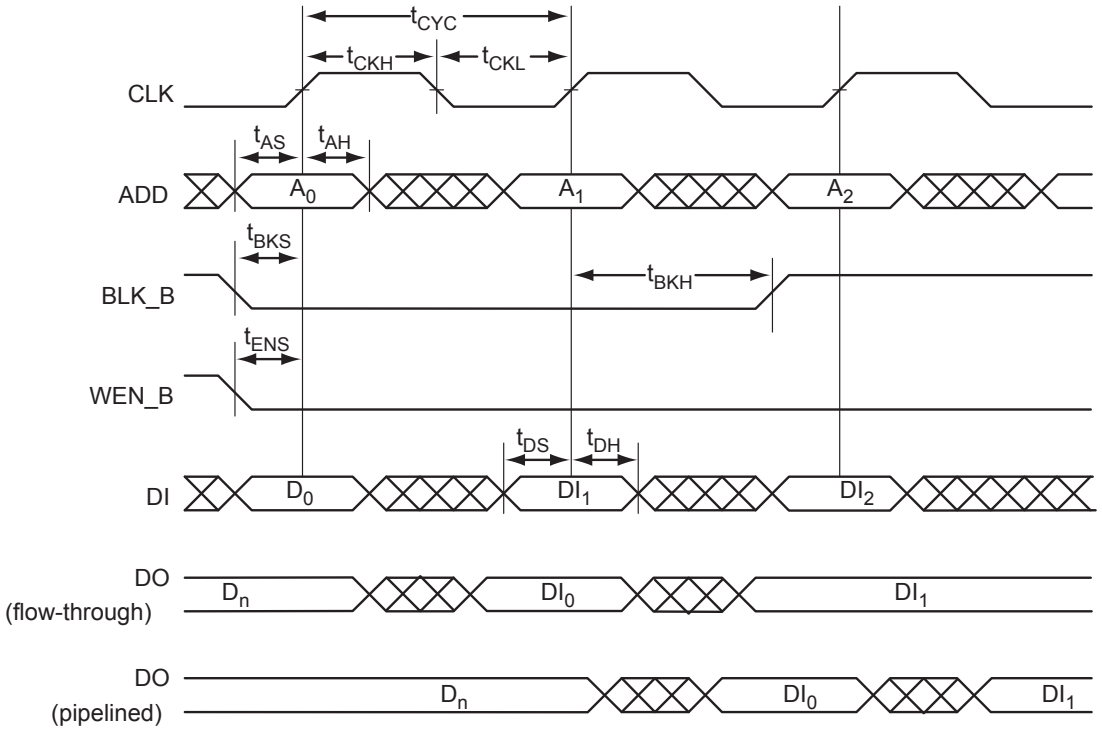


Figure 2-53 • **RAM Write, Output as Write Data (WMODE = 1)**

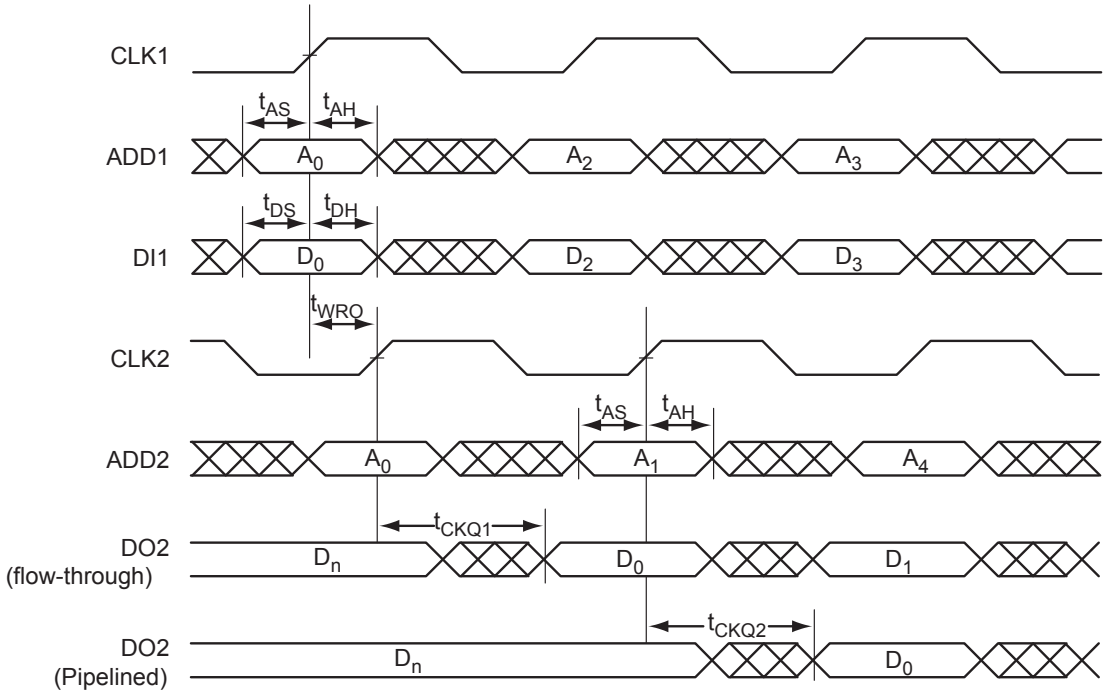


Figure 2-54 • **One Port Write / Other Port Read Same**

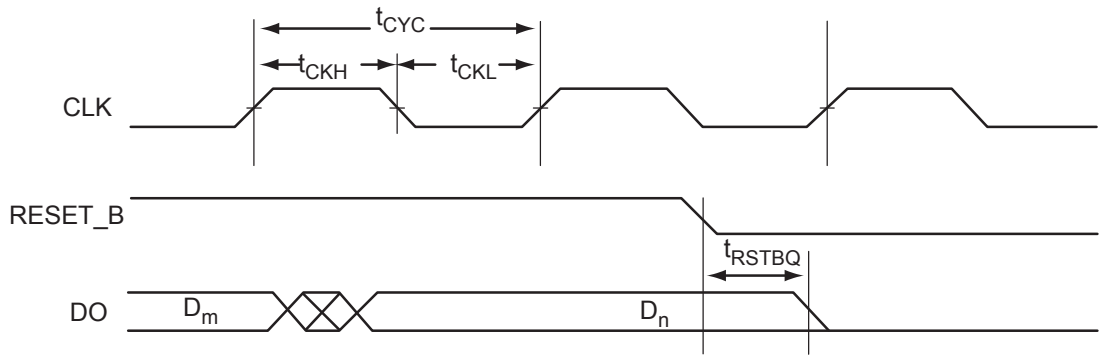


Figure 2-55 • **RAM Reset**

Timing Characteristics

Table 2-30 • RAM4K9, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.26	0.29	0.34	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B setup time	0.15	0.17	0.20	ns
t_{ENH}	REN_B, WEN_B hold time	0.10	0.11	0.13	ns
t_{BKS}	BLK_B setup time	0.24	0.27	0.32	ns
t_{BKH}	BLK_B hold time	0.02	0.02	0.03	ns
t_{DS}	Input data (DI) setup time	0.19	0.22	0.25	ns
t_{DH}	Input data (DI) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DO (output retained, WMODE = 0)	1.84	2.10	2.47	ns
	Clock High to new data valid on DO (flow-through, WMODE = 1)	2.43	2.77	3.25	ns
t_{CKQ2}	Clock High to new data valid on DO (pipelined)	0.92	1.05	1.23	ns
t_{C2CWWH}	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.23	0.26	0.30	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.34	0.38	0.45	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.37	0.42	0.49	ns
t_{RSTBQ}	RESET_B Low to data out Low on DO (flow-through)	0.95	1.08	1.27	ns
	RESET_B Low to Data Out Low on DO (pipelined)	0.95	1.08	1.27	ns
$t_{REMRSTB}$	RESET_B removal	0.29	0.34	0.39	ns
$t_{RECRSTB}$	RESET_B recovery	1.55	1.76	2.07	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.22	0.25	0.29	ns
t_{CYC}	Clock cycle time	3.33	3.79	4.46	ns
FMAX	Maximum frequency	300	264	224	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-31 • RAM512X18, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.26	0.29	0.34	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B setup time	0.09	0.11	0.13	ns
t_{ENH}	REN_B, WEN_B hold time	0.06	0.07	0.08	ns
t_{DS}	Input data (DI) setup time	0.19	0.22	0.25	ns
t_{DH}	Input data (DI) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DO (output retained, WMODE = 0)	2.23	2.54	2.98	ns
t_{CKQ2}	Clock High to new data valid on DO (pipelined)	0.92	1.05	1.24	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.38	0.43	0.50	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.44	0.50	0.59	ns
t_{RSTBQ}	RESET_B Low to data out Low on DO (flow-through)	0.95	1.08	1.27	ns
	RESET_B Low to data out Low on DO (pipelined)	0.95	1.08	1.27	ns
$t_{REMRSTB}$	RESET_B removal	0.29	0.34	0.39	ns
$t_{RECRSTB}$	RESET_B recovery	1.55	1.76	2.07	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.22	0.25	0.29	ns
t_{CYC}	Clock cycle time	3.33	3.79	4.46	ns
FMAX	Maximum frequency	300	264	224	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

FIFO4K18 Description

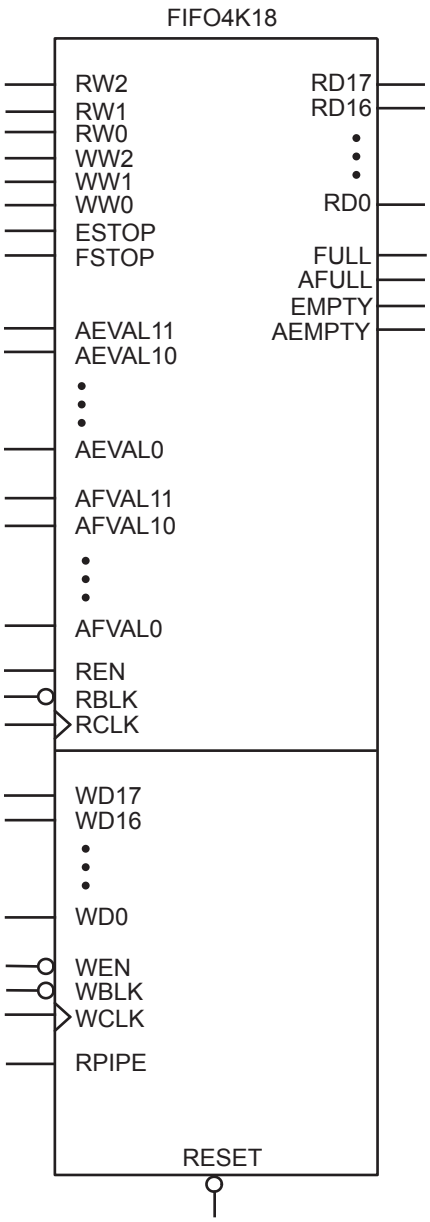


Figure 2-56 • **FIFO4KX18**

The following signals are used to configure the FIFO4K18 memory element:

WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 2-32).

Table 2-32 • Aspect Ratio Settings for WW[2:0]

WW2, WW1, WW0	RW2, RW1, RW0	D×W
000	000	4k×1
001	001	2k×2
010	010	1k×4
011	011	512×9
100	100	256×18
101, 110, 111	101, 110, 111	Reserved

WBLK and RBLK

These signals are active low and will enable the respective ports when Low. When the RBLK signal is High, the corresponding port's outputs hold the previous value.

WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

RPIPE

This signal is used to specify pipelined read on the output. A Low on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

RESET

This active low signal resets the output to zero when asserted. It resets the FIFO counters. It also sets all the RD pins Low, the FULL and AFULL pins Low, and the EMPTY and AEMPTY pins High (Table 2-33).

Table 2-33 • Input Data Signal Usage for Different Aspect Ratios

D×W	WD/RD Unused
4k×1	WD[17:1], RD[17:1]
2k×2	WD[17:2], RD[17:2]
1k×4	WD[17:4], RD[17:4]
512×9	WD[17:9], RD[17:9]
256×18	–

WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 2-33).

RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 2-33).

ESTOP, FSTOP

ESTOP is used to stop the FIFO read counter from further counting once the FIFO is empty (i.e., the EMPTY flag goes High). A High on this signal inhibits the counting.

FSTOP is used to stop the FIFO write counter from further counting once the FIFO is full (i.e., the FULL flag goes High). A High on this signal inhibits the counting.

For more information on these signals, refer to the "ESTOP and FSTOP Usage" section.

FULL, EMPTY

When the FIFO is full and no more data can be written, the FULL flag asserts High. The FULL flag is synchronous to WCLK to inhibit writing immediately upon detection of a full condition and to prevent overflows. Since the write address is compared to a resynchronized (and thus time-delayed) version of the read address, the FULL flag will remain asserted until two WCLK active edges after a read operation eliminates the full condition.

When the FIFO is empty and no more data can be read, the EMPTY flag asserts High. The EMPTY flag is synchronous to RCLK to inhibit reading immediately upon detection of an empty condition and to prevent underflows. Since the read address is compared to a resynchronized (and thus time-delayed) version of the write address, the EMPTY flag will remain asserted until two RCLK active edges after a write operation removes the empty condition.

For more information on these signals, refer to the "FIFO Flag Usage Considerations" section on page 2-71.

AFULL, AEMPTY

These are programmable flags and will be asserted on the threshold specified by AFVAL and AEVAL, respectively.

When the number of words stored in the FIFO reaches the amount specified by AEVAL while reading, the AEMPTY output will go High. Likewise, when the number of words stored in the FIFO reaches the amount specified by AFVAL while writing, the AFULL output will go High.

AFVAL, AEVAL

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values, respectively. They are 12-bit signals. For more information on these signals, refer to "FIFO Flag Usage Considerations" section on page 2-71.

ESTOP and FSTOP Usage

The ESTOP pin is used to stop the read counter from counting any further once the FIFO is empty (i.e., the EMPTY flag goes High). Likewise, the FSTOP pin is used to stop the write counter from counting any further once the FIFO is full (i.e., the FULL flag goes High).

The FIFO counters in the Fusion device start the count at 0, reach the maximum depth for the configuration (e.g., 511 for a 512×9 configuration), and then restart at 0. An example application for the ESTOP, where the read counter keeps counting, would be writing to the FIFO once and reading the same content over and over without doing another write.

FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values, respectively. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

FIFO Characteristics

Timing Waveforms

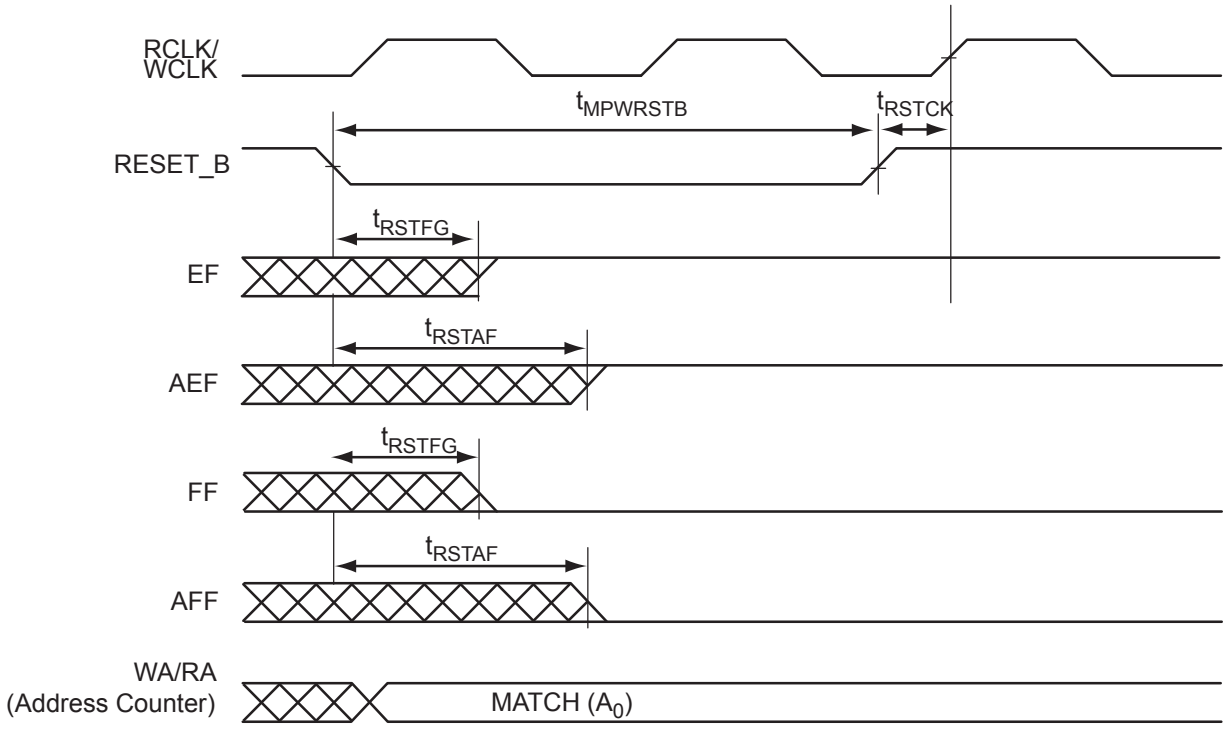


Figure 2-57 • **FIFO Reset**

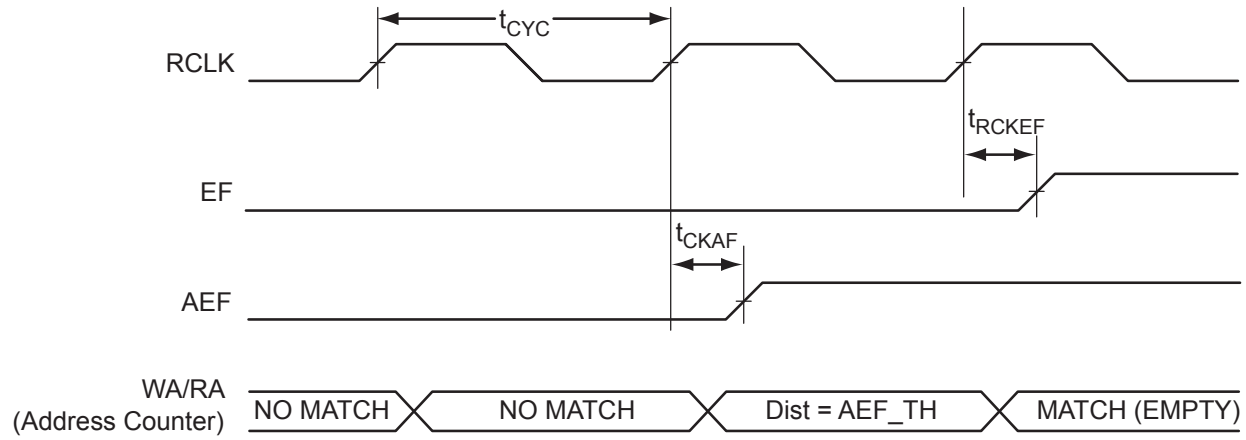


Figure 2-58 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

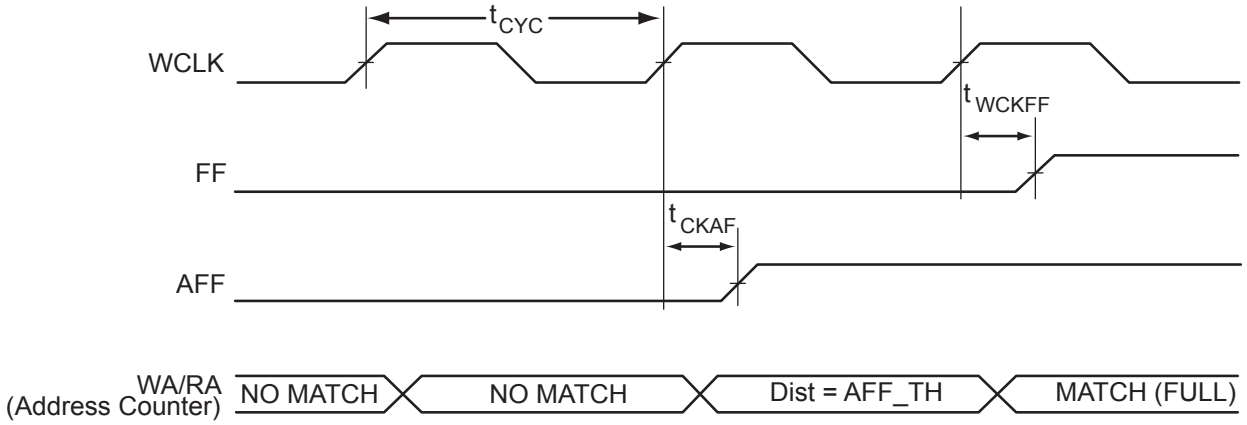


Figure 2-59 • **FIFO FULL and AFULL Flag Assertion**

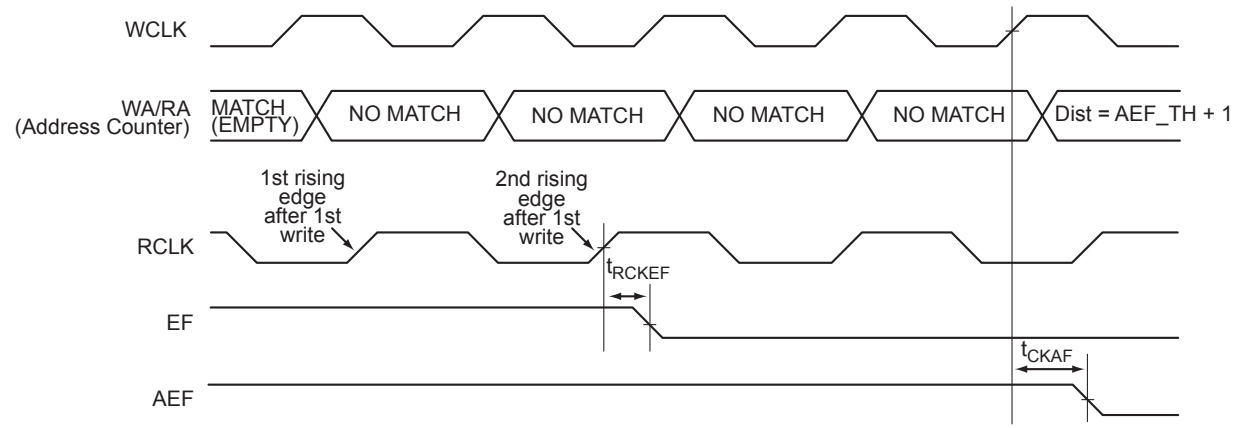


Figure 2-60 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

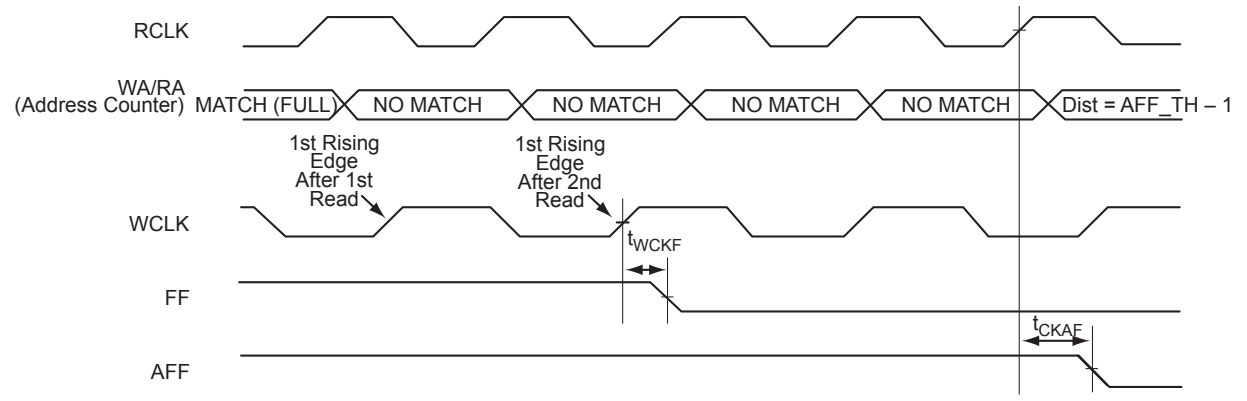


Figure 2-61 • **FIFO FULL Flag and AFULL Flag Deassertion**

Timing Characteristics

Table 2-34 • FIFO, Worst Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN_B, WEN_B Setup time	5.01	5.70	6.70	ns
t_{ENH}	REN_B, WEN_B Hold time	0.02	0.02	0.03	ns
t_{BKS}	BLK_B Setup time	0.19	0.22	0.26	ns
t_{BKH}	BLK_B Hold time	0.00	0.00	0.00	ns
t_{DS}	Input data (DI) Setup time	0.19	0.22	0.25	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (flow-through)	2.43	2.77	3.25	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	0.92	1.05	1.23	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.77	2.02	2.37	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.68	1.92	2.25	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.38	7.27	8.55	ns
t_{RSTFG}	RESET_B Low to Empty/Full Flag Valid	1.75	1.99	2.34	ns
t_{RSTAF}	RESET_B Low to Almost-Empty/Full Flag Valid	6.32	7.20	8.46	ns
t_{RSTBQ}	RESET_B Low to Data out Low on DO (flow-through)	0.95	1.08	1.27	ns
	RESET_B Low to Data out Low on DO (pipelined)	0.95	1.08	1.27	ns
$t_{REMRSTB}$	RESET_B Removal	0.29	0.34	0.39	ns
$t_{RECRSTB}$	RESET_B Recovery	1.55	1.76	2.07	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.22	0.25	0.29	ns
t_{CYC}	Clock Cycle time	3.33	3.79	4.46	ns
FMAX	Maximum Frequency for FIFO	300	264	224	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10 for derating values.

Analog Block

With the Fusion family, Actel has introduced the world's first mixed-mode FPGA solution. Supporting a robust analog peripheral mix, Fusion devices will support a wide variety of applications. It is this Analog Block that separates Fusion from all other FPGA solutions on the market today.

By combining both flash and high-speed CMOS processes in a single chip, these devices offer the best of both worlds. The high-performance CMOS is used for building RAM resources. These high-performance structures support device operation up to 350 MHz. Additionally, the advanced Actel 0.13 µm flash process incorporates high-voltage transistors and a high-isolation, triple-well process. Both of these are suited for the flash-based programmable logic and nonvolatile memory structures.

High-voltage transistors support the integration of analog technology in several ways. They aid in noise immunity so that the analog portions of the chip can be better isolated from the digital portions, increasing analog accuracy. Because they support high voltages, Actel flash FPGAs can be connected directly to high-voltage input signals, eliminating the need for external resistor divider networks, reducing component count, and increasing accuracy. By supporting higher internal voltages, the Actel advanced flash process enables high dynamic range on analog circuitry, increasing precision and signal–noise ratio. Actel flash FPGAs also drive high-voltage outputs, eliminating the need for external level shifters and drivers.

The unique triple-well process enables the integration of high-performance analog features with increased noise immunity and better isolation. By increasing the efficiency of analog design, the triple-well process also enables a smaller overall design size, reducing die size and cost.

The Analog Block consists of the Analog Quad I/O structure, RTC (for details refer to the "Real-Time Counter System" section on page 2-31), ADC, and ACM. All of these elements are combined in the single Analog Block macro, with which the user implements this functionality (Figure 2-62).

The Analog Block needs to be reset/reinitialized after the core powers up or the device is programmed. An external reset/initialize signal, which can come from the internal voltage regulator when it powers up, must be applied.

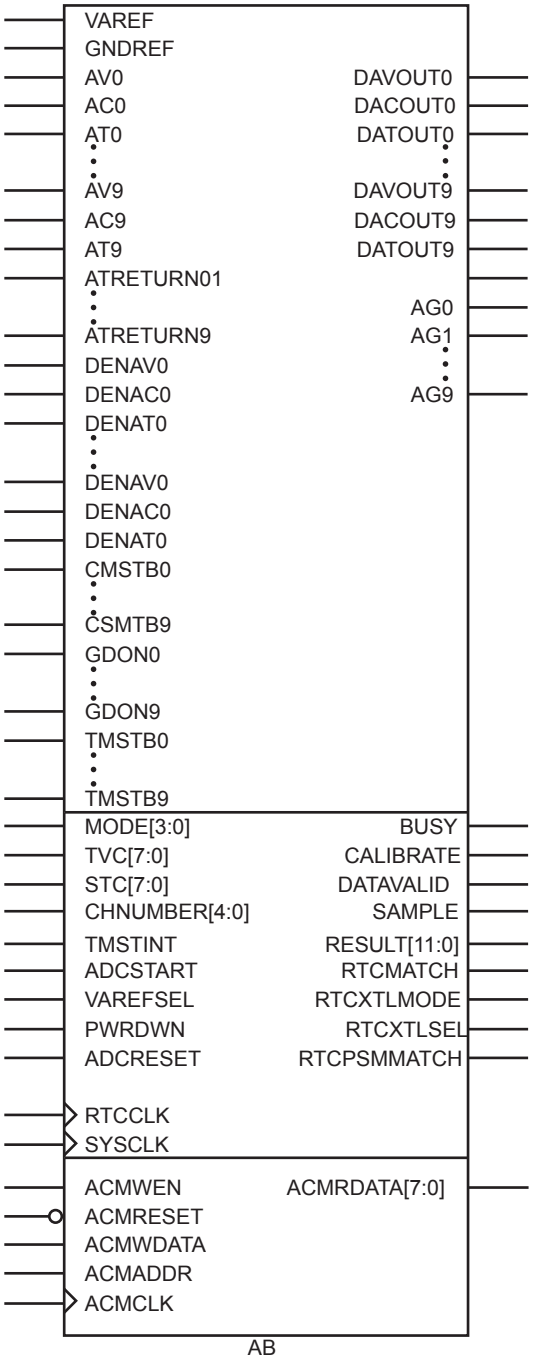


Figure 2-62 • **Analog Block Macro**

Table 2-35 describes each pin in the Analog Block. Each function within the Analog Block will be explained in detail in the following sections.

Table 2-35 • **Analog Block Pin Description**

Signal Name	Number of Bits	Direction	Function	Location of Details
VAREF	1	Input/Output	Voltage reference for ADC	ADC
GNDREF	1	Input	External ground reference	ADC
MODE[3:0]	4	Input	ADC operating mode	ADC
SYSCLK	1	Input	External system clock	
TVC[7:0]	8	Input	Clock divide control	ADC
STC[7:0]	8	Input	Sample time control	ADC
ADCSTART	1	Input	Start of conversion	ADC
PWRDWN	1	Input	ADC comparator power-down if 1. When asserted, the ADC will stop functioning, and the digital portion of the analog block will continue operating. This may result in invalid status flags from the analog block. Therefore, Actel does not recommend asserting the PWRDWN pin.	ADC
ADCRESET	1	Input	ADC resets and disables Analog Quad – active high	ADC
BUSY	1	Output	1 – Running conversion	ADC
CALIBRATE	1	Output	1 – Power-up calibration	ADC
DATAVALID	1	Output	1 – Valid conversion result	ADC
RESULT[11:0]	12	Output	Conversion result	ADC
TMSTBINT	1	Input	Internal temp. monitor strobe	ADC
SAMPLE	1	Output	1 – An analog signal is actively being sampled (stays high during signal acquisition only) 0 – No analog signal is being sampled	ADC
VAREFSEL	1	Input	0 = Output internal voltage reference (2.56 V) to VAREF 1 = Input external voltage reference from VAREF and GNDREF	ADC
CHNUMBER[4:0]	5	Input	Analog input channel select	Input multiplexer
ACMCLK	1	Input	ACM clock	ACM
ACMWEN	1	Input	ACM write enable – active high	ACM
ACMRESET	1	Input	ACM reset – active low	ACM
ACMWDATA[7:0]	8	Input	ACM write data	ACM
ACMRDATA[7:0]	8	Output	ACM read data	ACM
ACMADDR[7:0]	8	Input	ACM address	ACM
CMSTB0 to CMSTB9	10	Input	Current monitor strobe – 1 per quad, active high	Analog Quad

Table 2-35 • **Analog Block Pin Description (continued)**

Signal Name	Number of Bits	Direction	Function	Location of Details
GDON0 to GDON9	10	Input	Control to power MOS – 1 per quad	Analog Quad
TMSTB0 to TMSTB9	10	Input	Temperature monitor strobe – 1 per quad; active high	Analog Quad
DAVOUT0, DACOUT0, DATOUT0 to DAVOUT9, DACOUT9, DATOUT9	30	Output	Digital outputs – 3 per quad	Analog Quad
DENAV0, DENAC0, DENAT0 to DENAV9, DENAC9, DENAT9	30	Input	Digital input enables – 3 per quad	Analog Quad
AV0	1	Input	Analog Quad 0	Analog Quad
AC0	1	Input		Analog Quad
AG0	1	Output		Analog Quad
AT0	1	Input		Analog Quad
ATRETURN01	1	Input	Temperature monitor return shared by Analog Quads 0 and 1	Analog Quad
AV1	1	Input	Analog Quad 1	Analog Quad
AC1	1	Input		Analog Quad
AG1	1	Output		Analog Quad
AT1	1	Input		Analog Quad
AV2	1	Input	Analog Quad 2	Analog Quad
AC2	1	Input		Analog Quad
AG2	1	Output		Analog Quad
AT2	1	Input		Analog Quad
ATRETURN23	1	Input	Temperature monitor return shared by Analog Quads 2 and 3	Analog Quad
AV3	1	Input	Analog Quad 3	Analog Quad
AC3	1	Input		Analog Quad
AG3	1	Output		Analog Quad
AT3	1	Input		Analog Quad
AV4	1	Input	Analog Quad 4	Analog Quad
AC4	1	Input		Analog Quad
AG4	1	Output		Analog Quad
AT4	1	Input		Analog Quad
ATRETURN45	1	Input	Temperature monitor return shared by Analog Quads 4 and 5	Analog Quad
AV5	1	Input	Analog Quad 5	Analog Quad
AC5	1	Input		Analog Quad
AG5	1	Output		Analog Quad
AT5	1	Input		Analog Quad
AV6	1	Input	Analog Quad 6	Analog Quad
AC6	1	Input		Analog Quad

Table 2-35 • **Analog Block Pin Description (continued)**

Signal Name	Number of Bits	Direction	Function	Location of Details
AG6	1	Output		Analog Quad
AT6	1	Input		Analog Quad
ATRETURN67	1	Input	Temperature monitor return shared by Analog Quads 6 and 7	Analog Quad
AV7	1	Input	Analog Quad 7	Analog Quad
AC7	1	Input		Analog Quad
AG7	1	Output		Analog Quad
AT7	1	Input		Analog Quad
AV8	1	Input	Analog Quad 8	Analog Quad
AC8	1	Input		Analog Quad
AG8	1	Output		Analog Quad
AT8	1	Input		Analog Quad
ATRETURN89	1	Input	Temperature monitor return shared by Analog Quads 8 and 9	Analog Quad
AV9	1	Input	Analog Quad 9	Analog Quad
AC9	1	Input		Analog Quad
AG9	1	Output		Analog Quad
AT9	1	Input		Analog Quad
RTCMATCH	1	Output	MATCH	RTC
RTCPSMMATCH	1	Output	MATCH connected to VRPSM	RTC
RTCXTLMODE[1:0]	2	Output	Drives XTLOSC RTCMODE[1:0] pins	RTC
RTCXTLSEL	1	Output	Drives XTLOSC MODESEL pin	RTC
RTCCLK	1	Input	RTC clock input	RTC

Analog Quad

With the Fusion family, Actel introduces the Analog Quad, shown in Figure 2-63 on page 2-80, as the basic analog I/O structure. The Analog Quad is a four-channel system used to precondition a set of analog signals before sending it to the ADC for conversion into a digital signal. To maximize the usefulness of the Analog Quad, the analog input signals can also be configured as LVTTL digital input signals. The Analog Quad is divided into four sections.

The first section is called the Voltage Monitor Block, and its input pin is named AV. It contains a two-channel analog multiplexer that allows an incoming analog signal to be routed directly to the ADC or allows the signal to be routed to a prescaler circuit before being sent to the ADC. The prescaler can be configured to accept analog signals between –12 V and 0 or between 0 and +12 V. The prescaler circuit scales the voltage applied to the ADC input pad such that it is compatible with the ADC input voltage range. The AV pin can also be used as a digital input pin.

The second section of the Analog Quad is called the Current Monitor Block. Its input pin is named AC. The Current Monitor Block contains all the same functions as the Voltage Monitor Block with one addition, which is a current monitoring function. A small external current sensing resistor (typically less than 1 Ω) is connected between the AV and AC pins and is in series with a power source. The Current Monitor Block contains a current monitor circuit that converts the current through the external resistor to a voltage that can then be read using the ADC.

The third part of the Analog Quad is called the Gate Driver Block, and its output pin is named AG. This section is used to drive an external FET. There are two modes available: a High Current Drive mode and a Current Source Control mode. Both negative and positive voltage polarities are available, and in the current source control mode, four different current levels are available.

The fourth section of the Analog Quad is called the Temperature Monitor Block, and its input pin name is AT. This block is similar to the Voltage Monitor Block, except that it has an additional function: it can be used to monitor the temperature of an external diode-connected transistor. It has a modified prescaler and is limited to positive voltages only.

The Analog Quad can be configured during design time by Actel Libero IDE; however, the ACM can be used to change the parameters of any of these I/Os during runtime. This type of change is referred to as a context switch. The Analog Quad is a modular structure that is replicated to generate the analog I/O resources. Each Fusion device supports between 5 and 10 Analog Quads.

The analog pads are numbered to clearly identify both the type of pad (voltage, current, gate driver, or temperature pad) and its corresponding Analog Quad (AV0, AC0, AG0, AT0, AV1, …, AC9, AG9, and AT9). There are three types of input pads (AVx, ACx, and ATx) and one type of analog output pad (AGx). Since there can be up to 10 Analog Quads on a device, there can be a maximum of 30 analog input pads and 10 analog output pads.

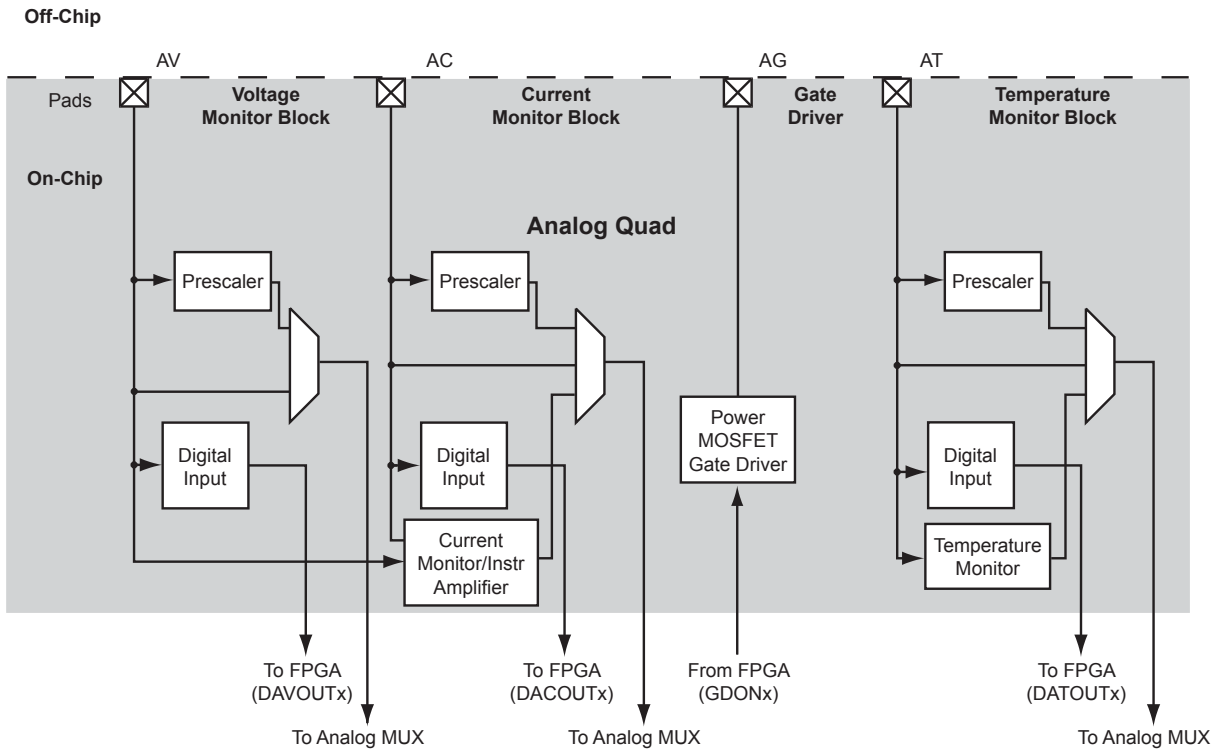


Figure 2-63 • **Analog Quad**

Voltage Monitor

The Fusion Analog Quad offers a robust set of voltage-monitoring capabilities unique in the FPGA industry. The Analog Quad comprises three analog input pads—Analog Voltage (AV), Analog Current (AC), and Analog Temperature (AT)—and a single gate driver output pad, Analog Gate (AG). There are many common characteristics among the analog input pads. Each analog input can be configured to connect directly to the input MUX of the ADC. When configured in this manner (Figure 2-64), there will be no prescaling of the input signal. Care must be taken in this mode not to drive the ADC into saturation by applying an input voltage greater than the reference voltage. The internal reference voltage of the ADC is 2.56 V. Optionally, an external reference can be supplied by the user. The external reference can be a maximum of 3.3 V DC.

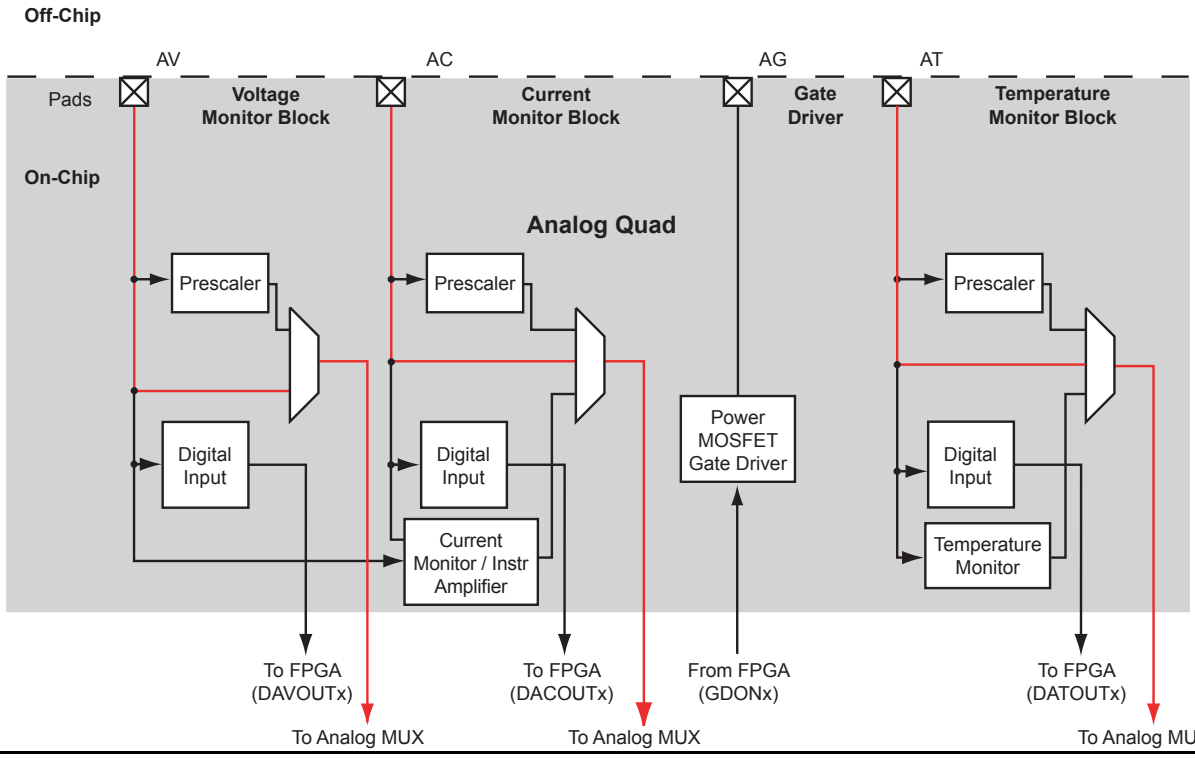


Figure 2-64 • **Analog Quad Direct Connect**

The Analog Quad offers a wide variety of prescaling options to enable the ADC to resolve the input signals. Figure 2-65 shows the path through the Analog Quad for a signal that is to be prescaled prior to conversion. The ADC internal reference voltage and the prescaler factors were selected to make both prescaling and postscaling of the signals easy binary calculations (refer to Table 2-54 on page 2-128 for details). When an analog input pad is configured with a prescaler, there will be a 1 MΩ resistor to ground. This occurs even when the device is in power-down mode. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, analog inputs are pulled down to ground through a 1 MΩ resistor. The gate driver output is floating (or tristated), and there is no extra current on VCC33A.

These scaling factors hold true whether the particular pad is configured to accept a positive or negative voltage. Note that whereas the AV and AC pads support the same prescaling factors, the AT pad supports a reduced set of prescaling factors and supports positive voltages only.

Typical scaling factors are given in Table 2-54 on page 2-128, and the gain error (which contributes to the minimum and maximum) is in Table 2-46 on page 2-114.

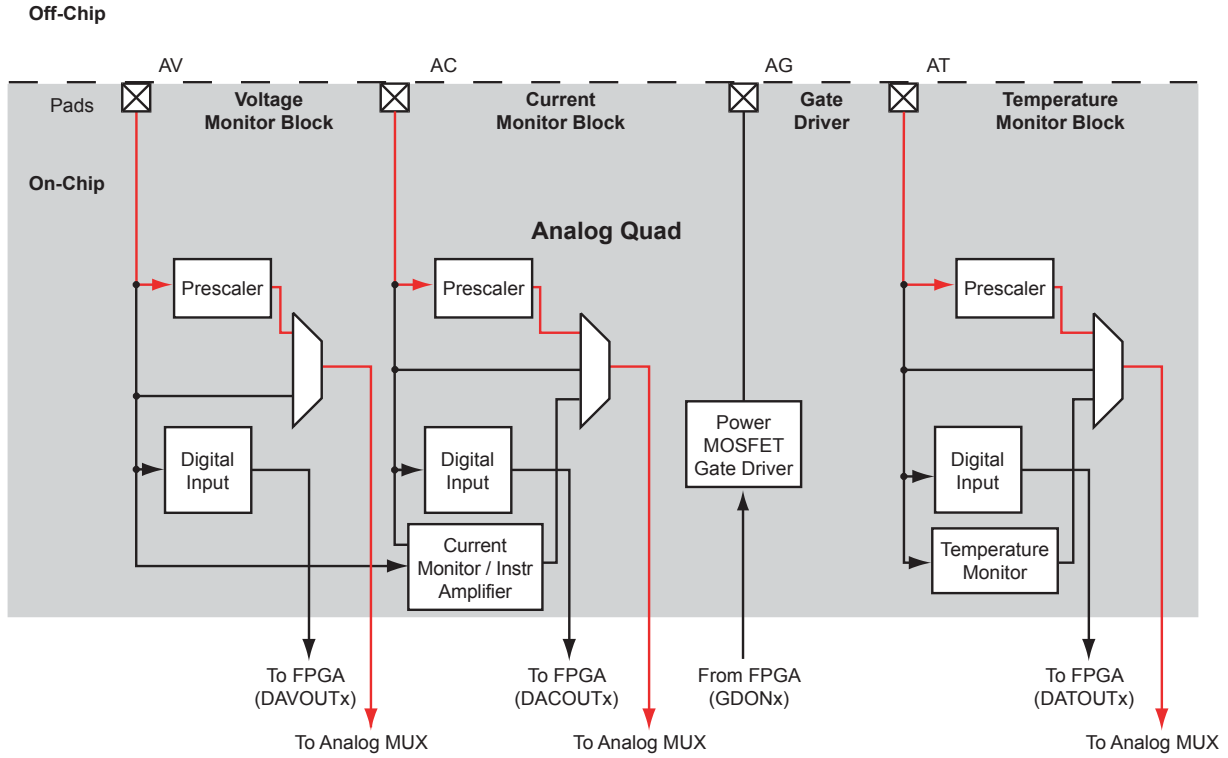


Figure 2-65 • **Analog Quad Prescaler Input Configuration**

Terminology

BW – Bandwidth

BW is a range of frequencies that a Channel can handle.

Channel

A channel is define as an analog input configured as one of the Prescaler range shown in Table 2-54 on page 2-128. The channel includes the Prescaler circuit and the ADC.

Channel Gain

Channel Gain is a measured of the deviation of the actual slope from the ideal slope. The slope is measured from the 20% and 80% point.

$$\text{Gain} = \frac{\text{Gain}_{\text{actual}}}{\text{Gain}_{\text{ideal}}}$$

EQ 1

Channel Gain Error

Channel Gain Error is a deviation from the ideal slope of the transfer function. The Prescaler Gain Error is expressed as the percent difference between the actual and ideal, as shown in EQ 2.

$$\text{Error}_{\text{Gain}} = (1 - \text{Gain}) \times 100\%$$

EQ 2

Channel Input Offset Error

Channel Offset error is measured as the input voltage that causes the transition from zero to a count of one. An Ideal Prescaler will have offset equal to one-half of the LSB voltage. Offset error is a positive or negative when the first transition point is higher or lower than ideal. Offset error is expressed in LSB or input voltage.

Total Channel Error

Total Channel Error is defined as the total error measured compared to the ideal value. Total Channel Error is the sum of gain error and offset error combined. Figure 2-66 shows how Total Channel Error is measured.

Total Channel Error is defined as the difference between the actual ADC output and ideal ADC output. In the example shown in Figure 2-66, the Total Channel Error would be a negative number.

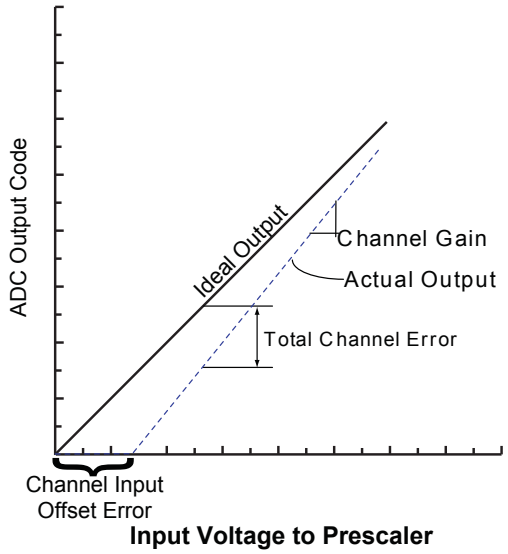


Figure 2-66 • **Total Channel Error Example**

Direct Digital Input

The AV, AC, and AT pads can also be configured as high-voltage digital inputs (Figure 2-67). As these pads are 12 V–tolerant, the digital input can also be up to 12 V. However, the frequency at which these pads can operate is limited to 10 MHz.

To enable one of these analog input pads to operate as a digital input, its corresponding Digital Input Enable (DENA*xy*) pin on the Analog Block must be pulled High, where *x* is either V, C, or T (for AV, AC, or AT pads, respectively) and *y* is in the range 0 to 9, corresponding to the appropriate Analog Quad.

When the pad is configured as a digital input, the signal will come out of the Analog Block macro on the appropriate DA*x*OUT*y* pin, where *x* represents the pad type (V for AV pad, C for AC pad, or T for AT pad) and *y* represents the appropriate Analog Quad number. Example: If the AT pad in Analog Quad 5 is configured as a digital input, it will come out on the DATOUT5 pin of the Analog Block macro.

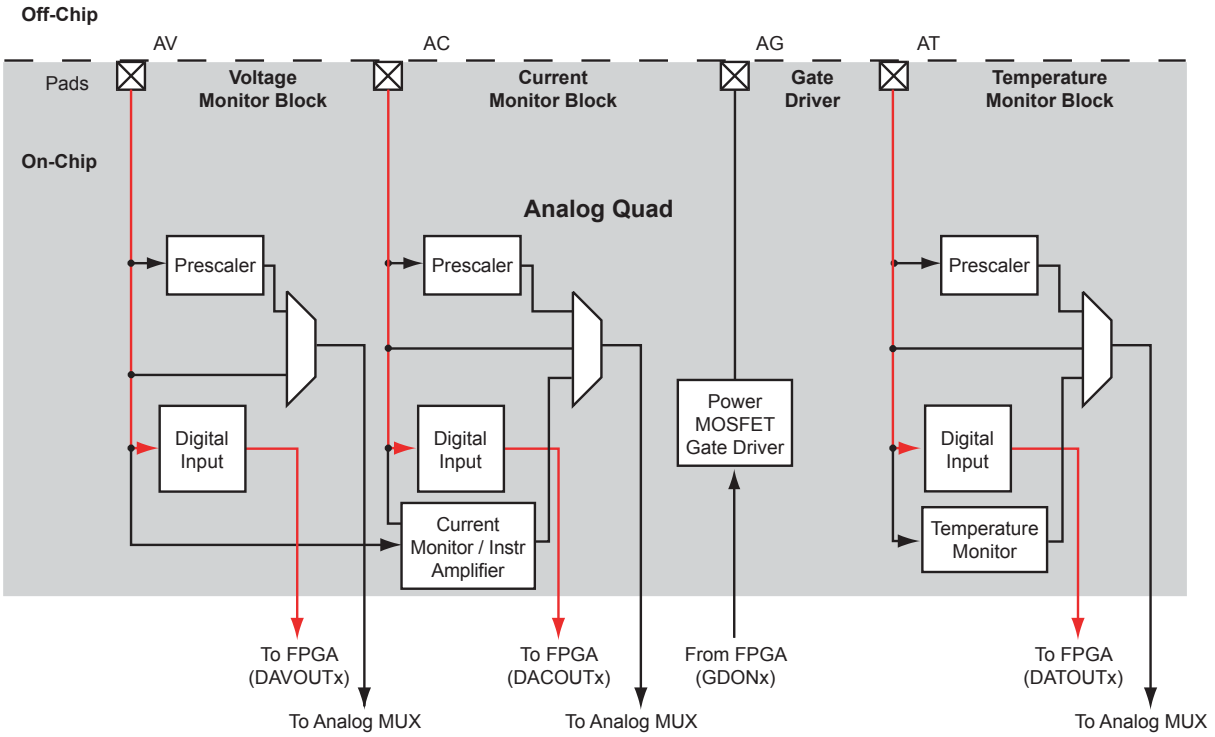


Figure 2-67 • **Analog Quad Direct Digital Input Configuration**

Current Monitor

The Fusion Analog Quad is an excellent element for voltage- and current-monitoring applications. In addition to supporting the same functionality offered by the AV pad, the AC pad can be configured to monitor current across an external sense resistor (Figure 2-68). To support this current monitor function, a differential amplifier with 10x gain passes the amplified voltage drop between the AV and AC pads to the ADC. The amplifier enables the user to use very small resistor values, thereby limiting any impact on the circuit. This function of the AC pad does not limit AV pad operation. The AV pad can still be configured for use as a direct voltage input or scaled through the AV prescaler independently of it's use as an input to the AC pad's differential amplifier.

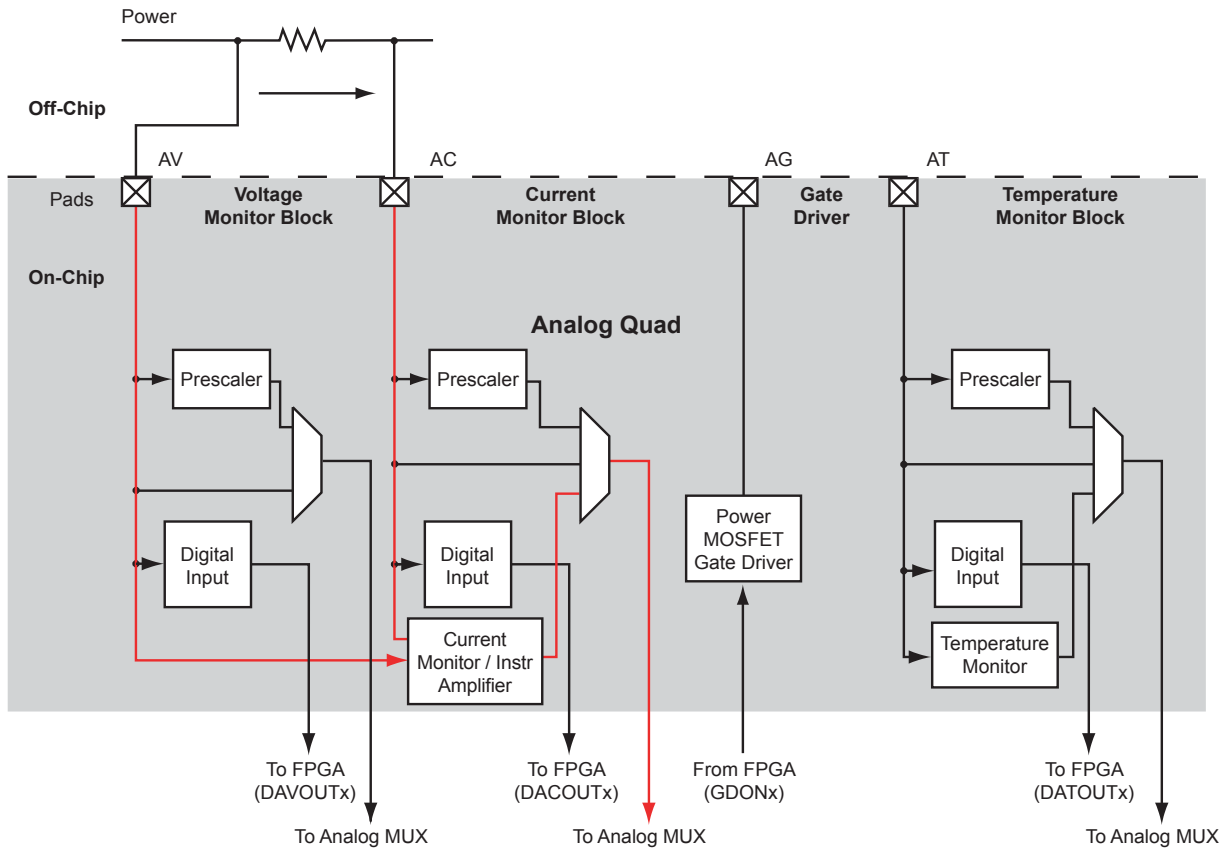


Figure 2-68 • **Analog Quad Current Monitor Configuration**

To initiate a current measurement, the appropriate Current Monitor Strobe (CMSTB) signal on the AB macro must be asserted low for at least t_{CMSLO} in order to discharge the previous measurement. Then CMSTB must be asserted high for at least t_{CMSET} prior to asserting the ADCSTART signal. The CMSTB must remain high until after the SAMPLE signal is deasserted by the AB macro. Note that the minimum sample time cannot be less than t_{CMSHI}. Figure 2-69 shows the timing diagram of CMSTB in relationship with the ADC control signals.

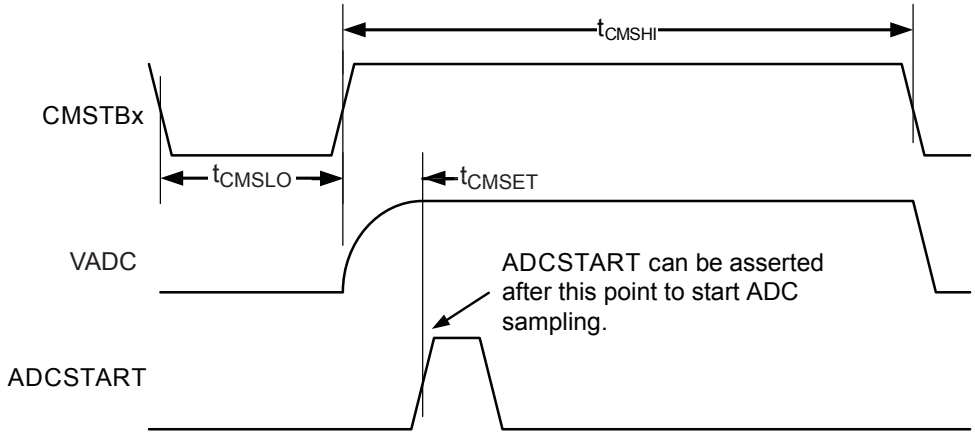


Figure 2-69 • **Timing Diagram for Current Monitor Strobe**

Figure 2-70 on page 2-87 illustrates positive current monitor operation. The differential voltage between AV and AC goes into the 10× amplifier and is then converted by the ADC. For example, a current of 1.5 A is drawn from a 10 V supply and is measured by the voltage drop across a 0.050 Ω sense resistor, The voltage drop is amplified by ten times by the amplifier and then measured by the ADC. The 1.5 A current creates a differential voltage across the sense resistor of 75 mV. This becomes 750 mV after amplification. Thus, the ADC measures a current of 1.5 A as 750 mV. Using an ADC with 8-bit resolution and VAREF of 2.56 V, the ADC result is decimal 75. EQ 3 shows how to compute the current from the ADC result.

$$|I| = (ADC \times V_{AREF}) / (10 \times 2^{N} \times R_{sense})$$

EQ 3

where

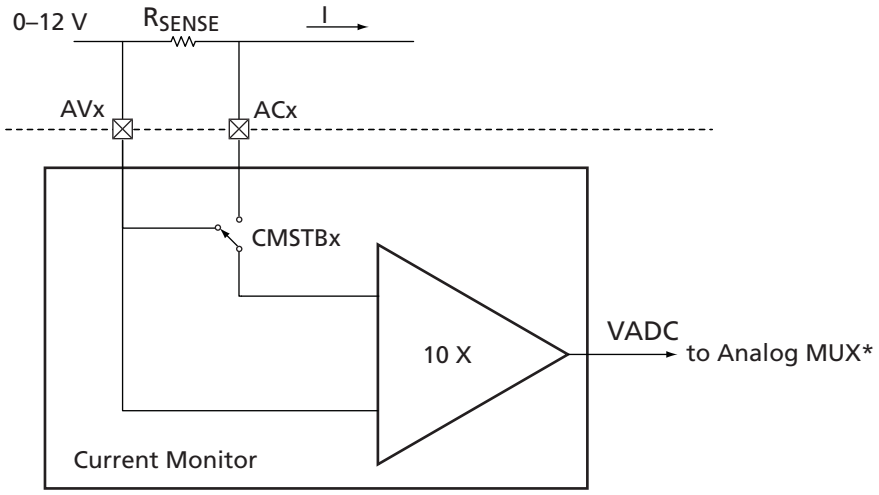
I is the current flowing through the sense resistor

ADC is the result from the ADC

VAREF is the Reference voltage

N is the number of bits

Rsense is the resistance of the sense resistor



*Note: *Refer to Table 2-38 on page 2-96 for the MUX channel number.*

Figure 2-70 • **Positive Current Monitor**

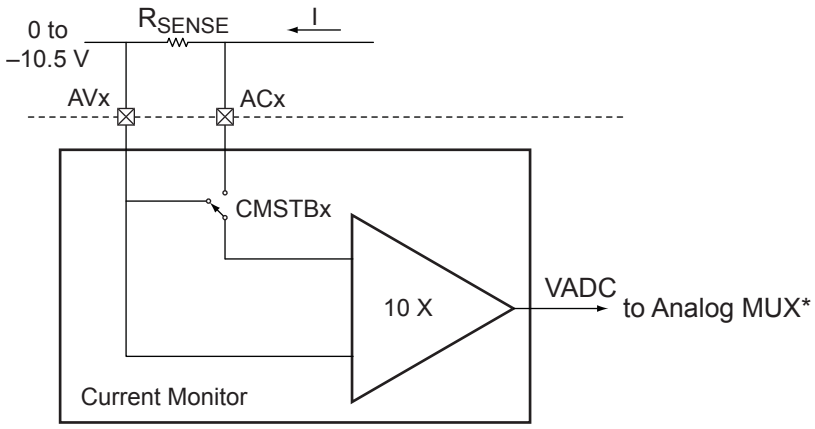
Care must be taken when choosing the right resistor for current measurement application. Note that because of the 10× amplification, the maximum measurable difference between the AV and AC pads is V_{AREF} / 10. A larger AV-to-AC voltage drop will result in ADC saturation; that is, the digital code put out by the ADC will stay fixed at the full scale value. Therefore, the user must select the external sense resistor appropriately. Table 2-36 on page 2-88 shows recommended resistor values for different current measurement ranges. When choosing resistor values for a system, there is a trade-off between measurement accuracy and power consumption. Choosing a large resistor will increase the voltage drop and hence increase accuracy of the measurement; however the larger voltage drop dissipates more power ($P = I^2 \times R$).

The Current Monitor is a unipolar system, meaning that the differential voltage swing must be from 0 V to VAREF/10. Therefore, the Current Monitor only supports differential voltage where |VAV-VAC| is greater than 0 V. This results in the requirement that the potential of the AV pad must be larger than the potential of the AC pad. This is straightforward for positive voltage systems. For a negative voltage system, it means that the AV pad must be "more negative" than the AC pad. This is shown in Figure 2-71 on page 2-88.

In this case, both the AV pad and the AC pad are configured for negative operations and the output of the differential amplifier still falls between 0 V and VAREF as required.

Table 2-36 • Recommended Resistor for Different Current Range Measurement

Current Range	Recommended Minimum Resistor Value (Ohms)
> 5 mA – 10 mA	10 – 20
> 10 mA – 20 mA	5 – 10
> 20 mA – 50 mA	2.5 – 5
> 50 mA – 100 mA	1 – 2
> 100 mA – 200 mA	0.5 – 1
> 200 mA – 500 mA	0.3 – 0.5
> 500 mA – 1 A	0.1 – 0.2
> 1 A – 2 A	0.05 – 0.1
> 2 A – 4 A	0.025 – 0.05
> 4 A – 8 A	0.0125 – 0.025
> 8 A – 12 A	0.00625 – 0.02



*Note: *Refer to Table 2-38 on page 2-96 for the MUX channel number.*

Figure 2-71 • Negative Current Monitor

Terminology

Accuracy

The accuracy of Fusion Current Monitor is ±2 mV minimum plus 5% of the differential voltage at the input. The input accuracy can be translated to error at the ADC output by using EQ 4. The 10 V/V gain is the gain of the Current Monitor Circuit, as described in the "Current Monitor" section on page 2-85. For 8-bit mode, $N = 8$, $V_{AREF} = 2.56$ V, zero differential voltage between AV and AC, the Error (E_{ADC}) is equal to 2 LSBs.

$$E_{ADC} = (2mV + 0.05|V_{AV} - V_{AC}|) \times (10V)/V \times \frac{2^N}{VAREF}$$

EQ 4

where

N is the number of bits

*V*AREF is the Reference voltage

V_{AV} is the voltage at AV pad

V_{AC} is the voltage at AC pad

Gate Driver

The Fusion Analog Quad includes a Gate Driver connected to the Quad's AG pin (Figure 2-72). Designed to work with external p- or n-channel MOSFETs, the Gate driver is a configurable current sink or source and requires an external pull-up or pull-down resistor. The AG supports 4 selectable gate drive levels: 1 µA, 3 µA, 10 µA, and 30 µA (Figure 2-73 on page 2-90). The AG also supports a High Current Drive mode in which it can sink 20 mA; in this mode the switching rate is approximately 1.3 MHz with 100 ns turn-on time and 600 ns turn-off time. Modeled on an open-drain-style output, it does not output a voltage level without an appropriate pull-up or pull-down resistor. If 1 V is forced on the drain, the current sinking/sourcing will exceed the ability of the transistor, and the device could be damaged.

The AG pad is turned on via the corresponding GDON*x* pin in the Analog Block macro, where *x* is the number of the corresponding Analog Quad for the AG pad to be enabled (GDON0 to GDON9).

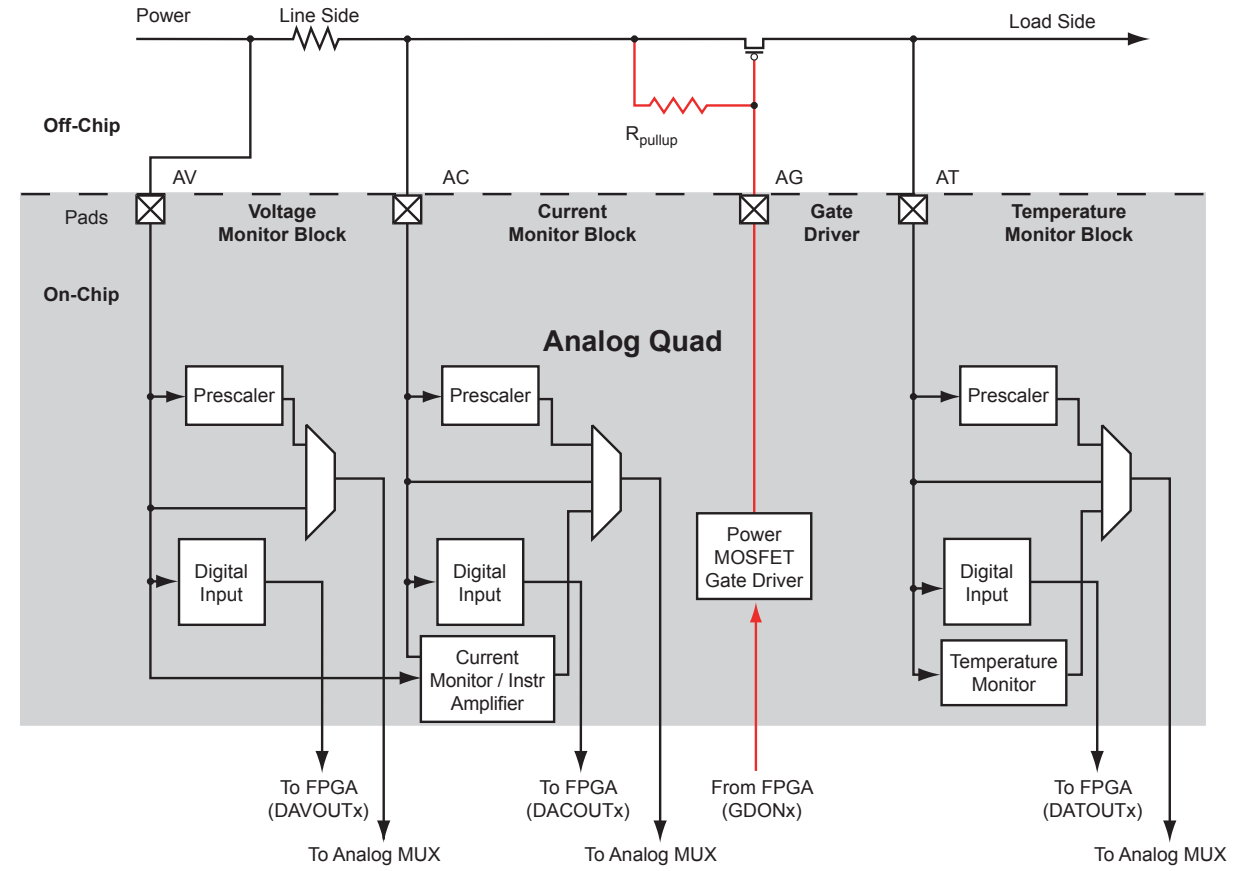


Figure 2-72 • **Gate Driver**

The gate-to-source voltage (V_{gs}) of the external MOSFET is limited to the programmable drive current times the external pull-up or pull-down resistor value (EQ 5).

$$V_{gs} \le I_g \times (R_{pullup} \text{ or } R_{pulldown})$$

EQ 5

The rate at which the gate voltage of the external MOSFET slews is determined by the current, I_g, sourced or sunk by the AG pin and the gate-to-source capacitance, C_{GS}, of the external MOSFET. As an approximation, the slew rate is given by EQ 6.

$$dv/dt = I_g / C_{GS}$$

EQ 6

C_{GS} is not a fixed capacitance but, depending on the circuitry connected to its drain terminal, can vary significantly during the course of a turn-on or turn-off transient. Thus, EQ 6 on page 2-89 can only be used for a first-order estimate of the switching speed of the external MOSFET.

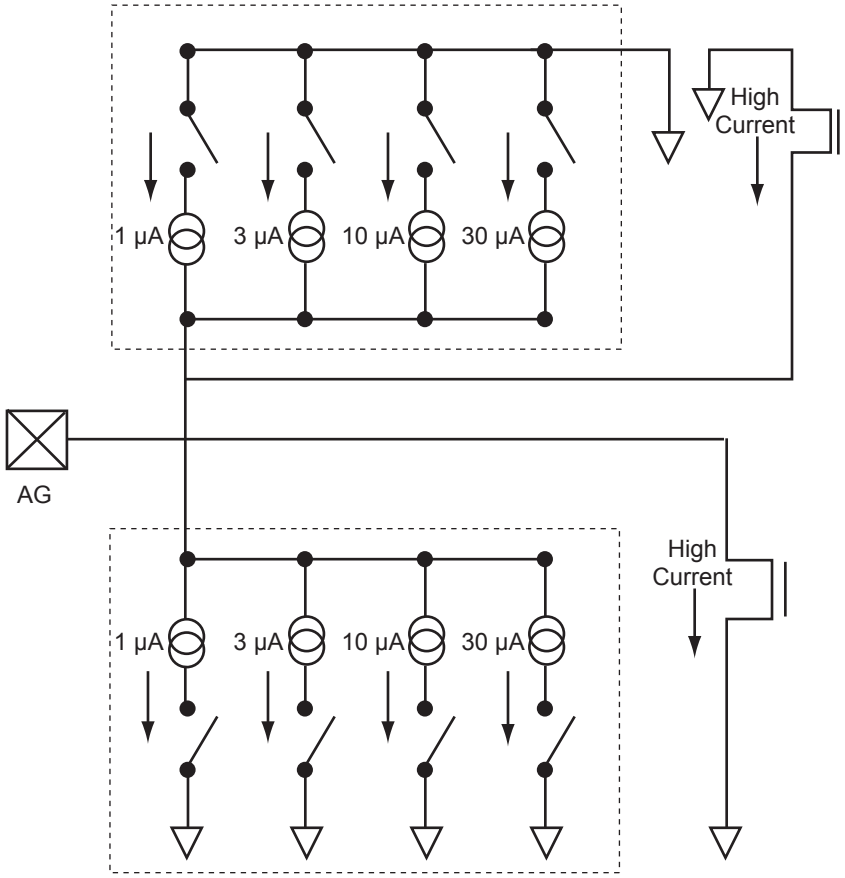


Figure 2-73 • **Gate Driver Example**

Temperature Monitor

The final pin in the Analog Quad is the Analog Temperature (AT) pin. The AT pin is used to implement an accurate temperature monitor in conjunction with an external diode-connected bipolar transistor (Figure 2-74). For improved temperature measurement accuracy, it is important to use the ATRTN pin for the return path of the current sourced by the AT pin. Each ATRTN pin is shared between two adjacent Analog Quads. Additionally, if not used for temperature monitoring, the AT pin can provide functionality similar to that of the AV pad. However, in this mode only positive voltages can be applied to the AT pin, and only two prescaler factors are available (16 V and 4 V ranges—refer to Table 2-54 on page 2-128).

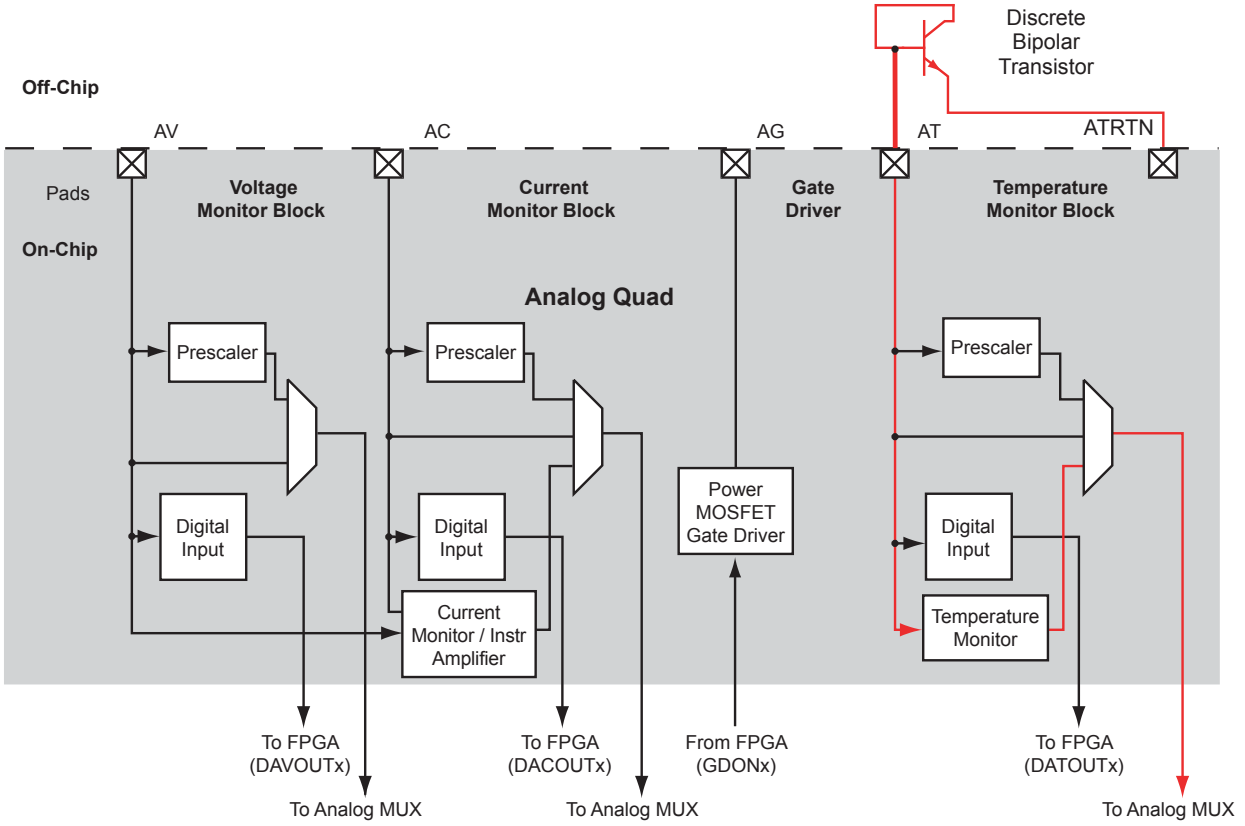
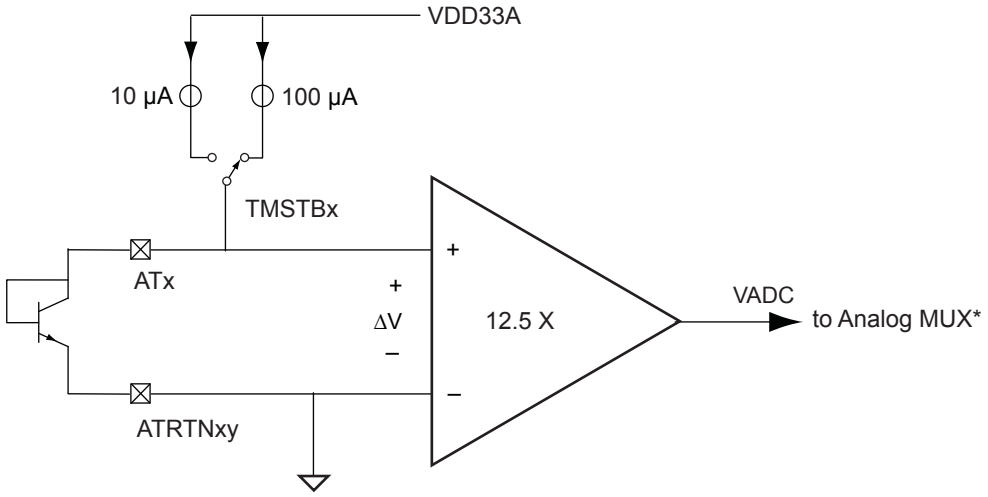


Figure 2-74 • **Temperature Monitor Quad**

Fusion uses a remote diode as a temperature sensor. The Fusion Temperature Monitor uses a differential input; the AT pin and ATRTN (AT Return) pin are the differential inputs to the Temperature Monitor. There is one Temperature Monitor in each Quad. A simplified block diagram is shown in Figure 2-75.



*Note: *Refer to Table 2-38 on page 2-96 for the MUX channel number.*

Figure 2-75 • **Block Diagram for Temperature Monitor Circuit**

The Fusion approach to measuring temperature is forcing two different currents through the diode with a ratio of 10:1. The switch that controls the different currents is controlled by the Temperature Monitor Strobe signal, TMSTB. Setting TMSTB to '1' will initiate a Temperature reading. The TMSTB should remain '1' until the ADC finishes sampling the voltage from the Temperature Monitor. The minimum sample time for the Temperature Monitor cannot be less than the minimum strobe high time minus the setup time. Figure 2-76 shows the timing diagram.

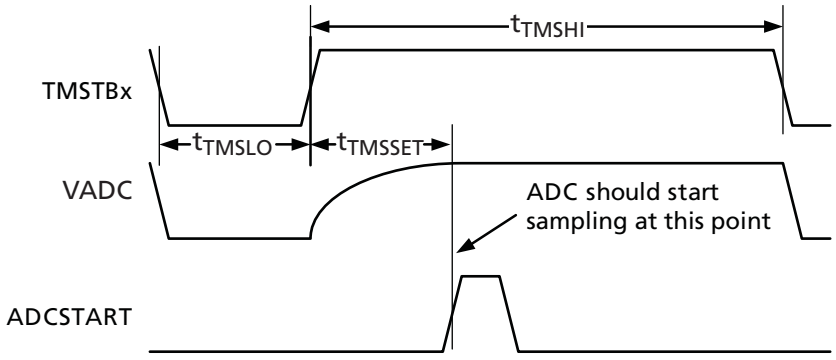


Figure 2-76 • **Timing Diagram for the Temperature Monitor Strobe Signal**

The diode's voltage is measured at each current level and the temperature is calculated based on EQ 7.

$$V_{TMSLO} - V_{TMSHI} = n\frac{kT}{q}\left(\ln\frac{I_{TMSLO}}{I_{TMSHI}}\right)$$

EQ 7

where

I_{TMSLO} is the current when the Temperature Strobe is Low, typically 100 µA

I_{TMSHI} is the current when the Temperature Strobe is High, typically 10 µA

V_{TMSLO} is diode voltage while Temperature Strobe is Low

V_{TMSHI} is diode voltage while Temperature Strobe is High

n is the non-ideality factor of the diode-connected transistor. It is typically 1.004 for the Actel-recommended transistor type 2N3904.

K = 1.3806 x 10^{-23} J/K is the Boltzman constant

Q = 1.602 x 10^{-19} C is the charge of a proton

When I_{TMSLO} / I_{TMSHI} = 10, the equation can be simplified as shown in EQ 8.

$$\Delta V = V_{TMSLO} - V_{TMSHI} = 1.986 \times 10^{-4} nT$$

EQ 8

In the Fusion TMB, the ideality factor n for 2N3904 is 1.004 and ΔV is amplified 12.5 times by an internal amplifier; hence the voltage before entering the ADC is as given in EQ 9.

$$V_{ADC} = \Delta V \times 12.5 = 2.5\ \text{mV}/(K \times T)$$

EQ 9

This means the temperature to voltage relationship is 2.5 mV per degree Kelvin. The unique design of Fusion has made the Temperature Monitor System simple for the user. When the 10-bit mode ADC is used, each LSB represents 1 degree Kelvin, as shown in EQ 10. That is, 25°C is equal to 293°K and is represented by decimal 293 counts from the ADC.

$$1K = 2.5\ \text{mV} \times \frac{2^{10}}{2.56\ \text{V}} = 1\ \text{LSB}$$

EQ 10

If 8-bit mode is used for the ADC resolution, each LSB represents 4 degrees Kelvin; however, the resolution remains as 1 degree Kelvin per LSB, even for 12-bit mode, due to the Temperature Monitor design. An example of the temperature data format for 10-bit mode is shown in Table 2-37.

Table 2-37 • **Temperature Data Format**

Temperature	Temperature (K)	Digital Output (ADC 10-bit mode)
–40°C	233	00 1110 1001
–20°C	253	00 1111 1101
0°C	273	01 0001 0001
1°C	274	01 0001 0010
10 °C	283	01 0001 1011
25°C	298	01 0010 1010
50 °C	323	01 0100 0011
85 °C	358	01 0110 0110

Terminology

Resolution

Resolution defines the smallest temperature change Fusion Temperature Monitor can resolve. For an ADC configured as 8-bit mode, each LSB represents 4°C, and 1°C per LSB for 10-bit mode. With 12-bit mode, the Temperature Monitor can still only resolve 1°C due to Temperature Monitor design.

Offset

The Fusion Temperature Monitor has a systematic offset of +11°C, excluding error due to board resistance and ideality factor of the external diode, between the operation range of –40°C to +85°C. For instance, 25°C will be read by the Temperature Monitor as 36°C plus error. The user can remove any offset error through hardware or software during the calibration routine.

Analog-to-Digital Converter Block

At the heart of the Fusion analog system is a programmable Successive Approximation Register (SAR) ADC. The ADC can support 8-, 10-, or 12-bit modes of operation. In 12-bit mode, the ADC can resolve 500 ksps. All results are MSB-justified in the ADC. The input to the ADC is a large 32:1 analog input multiplexer. A simplified block diagram of the Analog Quads, analog input multiplexer, and ADC is shown in Figure 2-77 on page 2-95. The ADC offers multiple self-calibrating modes to ensure consistent high performance both at power-up and during runtime.

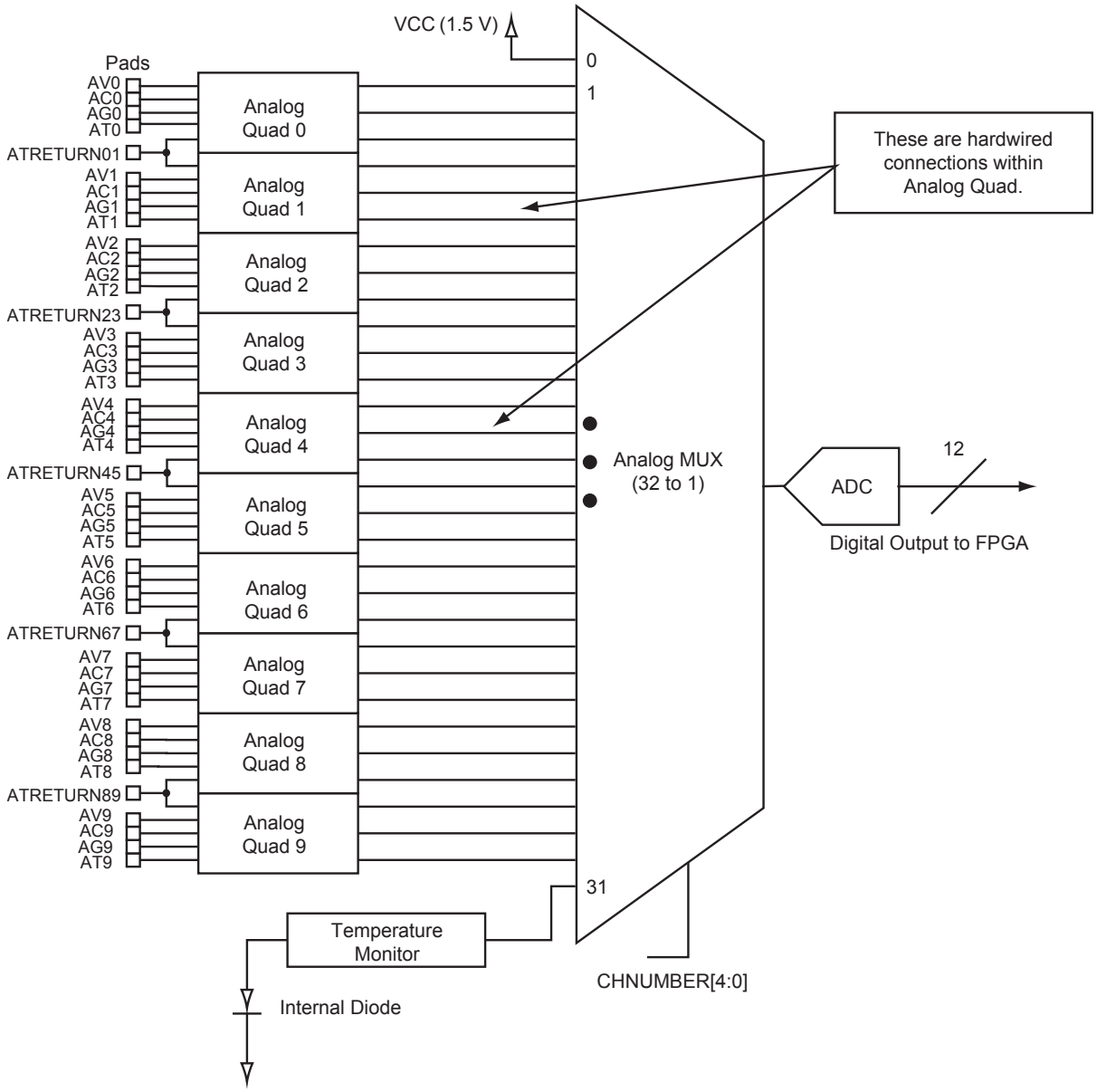


Figure 2-77 • **ADC Block Diagram**

ADC Input Multiplexer

At the input to the Fusion ADC is a 32:1 multiplexer. Of the 32 input channels, up to 30 are user definable. Two of these channels are hardwired internally. Channel 31 connects to an internal temperature diode so the temperature of the Fusion device itself can be monitored. Channel 0 is wired to the FPGA's 1.5 V VCC supply, enabling the Fusion device to monitor its own power supply. Doing this internally makes it unnecessary to use an analog I/O to support these functions. The balance of the MUX inputs are connected to Analog Quads (see the "Analog Quad" section on page 2-79). Table 2-38 defines which Analog Quad inputs are associated with which specific analog MUX channels. The number of Analog Quads present is device-dependent; refer to the family list in the "Fusion Extended Temperature Devices" table on page I of this datasheet for the number of quads per device. Regardless of the number of quads populated in a device, the internal connections to both VCC and the internal temperature diode remain on Channels 0 and 31, respectively. To sample the internal temperature monitor, it must be strobed (similar to the AT pads). The TMSTBINT pin on the Analog Block macro is the control for strobing the internal temperature measurement diode.

To determine which channel is selected for conversion, there is a five-pin interface on the Analog Block, CHNUMBER[4:0], defined in Table 2-39 on page 2-97. Table 2-38 shows the correlation between the analog MUX input channels and the analog input pins.

Table 2-38 • **Analog MUX Channels**

Analog MUX Channel	Signal	Analog Quad Number
0	Vcc_analog	
1	AV0	Analog Quad 0
2	AC0	
3	AT0	
4	AV1	Analog Quad 1
5	AC1	
6	AT1	
7	AV2	Analog Quad 2
8	AC2	
9	AT2	
10	AV3	Analog Quad 3
11	AC3	
12	AT3	
13	AV4	Analog Quad 4
14	AC4	
15	AT4	
16	AV5	Analog Quad 5
17	AC5	
18	AT5	
19	AV6	Analog Quad 6
20	AC6	
21	AT6	

Table 2-38 • **Analog MUX Channels (continued)**

Analog MUX Channel	Signal	Analog Quad Number
22	AV7	Analog Quad 7
23	AC7	
24	AT7	
25	AV8	Analog Quad 8
26	AC8	
27	AT8	
28	AV9	Analog Quad 9
29	AC9	
30	AT9	
31	Internal temperature monitor	

Table 2-39 • **Channel Selection**

Channel Number	CHNUMBER[4:0]
0	00000
1	00001
2	00010
3	00011
. . .	. . .
30	11110
31	11111

ADC Description

The Actel Fusion ADC is a 12-bit SAR ADC. It offers a wide variety of features for different use models. Figure 2-78 shows a block diagram of the Fusion ADC.

- Configurable resolution: 8-bit, 10-bit, and 12-bit mode
- DNL: 0.6 LSB for 10-bit mode
- INL: 0.4 LSB for 10-bit mode
- No missing code
- Internal VAREF = 2.56 V
- Maximum Sample Rate = 600 Ksps
- Power-up calibration and dynamic calibration after every sample to compensate for temperature drift over time

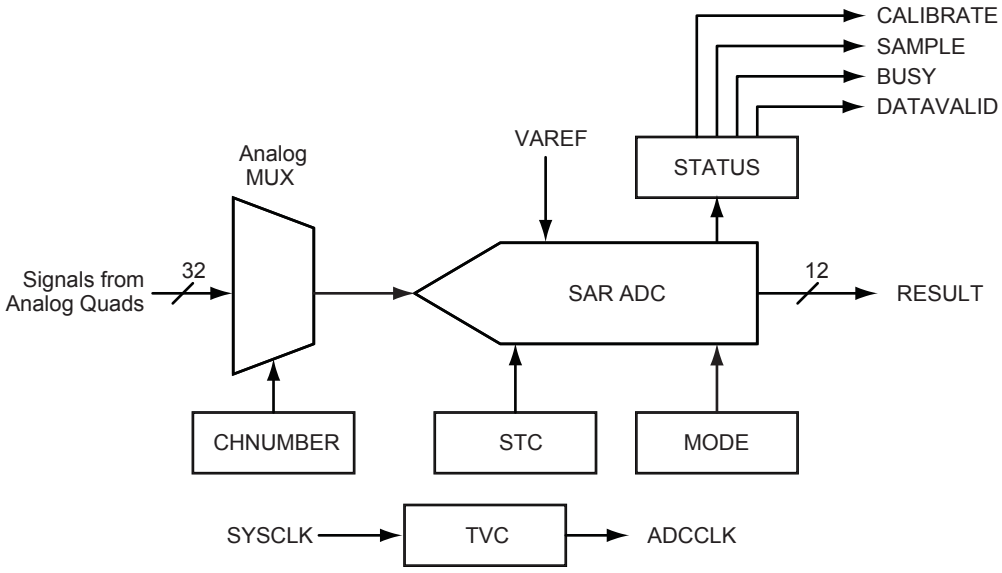


Figure 2-78 • **ADC Simplified Block Diagram**

ADC Configuration Description

The Fusion ADC can be configured to operate in 8-, 10-, or 12-bit modes, power-down after conversion, and dynamic calibration. This is controlled by MODE[3:0], as defined in Table 2-40.

The output of the ADC is the RESULT[11:0] signal. In 8-bit mode, the Most Significant 8 Bits RESULT[11:4] are used as the ADC value and the Least Significant 4 Bits RESULT[3:0] are logical '0's. In 10-bit mode, RESULT[11:2] are used the ADC value and RESULT[1:0] are logical '0's.

Table 2-40 • **Mode Bits Function**

Name	Bits	Function
MODE	3	0 – Internal calibration after every conversion; two ADCCLK cycles are used after the conversion. 1 – No calibration after every conversion
MODE	2	0 – Power-down after conversion 1 – No Power-down after conversion
MODE	1:0	00 – 10-bit 01 – 12-bit 10 – 8-bit 11 – Unused

The speed of the ADC depends on its internal clock, ADCCLK, which is not accessible to users. The ADCCLK is derived from SYSCLK. Input signal TVC[7:0], Time Divider Control, determines the speed of the ADCCLK in relationship to SYSCLK, based on EQ 11.

$$t_{ADCCLK} = 4 \times (1 + TVC) \times t_{SYSCLK}$$

EQ 11

TVC: Time Divider Control (0–255)

t_{ADCCLK} is the period of ADCCLK, and must be between 0.5 MHz and 10 MHz

t_{SYSCLK} is the period of SYSCLK

Table 2-41 • **TVC Bits Function**

Name	Bits	Function
TVC	[7:0]	SYSCLK divider control

The frequency of ADCCLK, f_{ADCCLK}, must be within 0.5 Hz to 10 MHz.

The inputs to the ADC are synchronized to SYSCLK. A conversion is initiated by asserting the ADCSTART signal on a rising edge of SYSCLK. Figure 2-80 on page 2-103 and Figure 2-81 on page 2-104 show the timing diagram for the ADC.

A conversion is performed in three phases. In the first phase, the analog input voltage is sampled on the input capacitor. This phase is called sample phase. During the sample phase, the output signals BUSY and SAMPLE change from '0' to '1', indicating the ADC is busy and sampling the analog signal. The sample time can be controlled by input signals STC[7:0]. The sample time can be calculated by EQ 12. When controlling the sample time for the ADC along with the use of Prescaler or Current Monitor or Temperature Monitor, the minimum sample time for each must be obeyed. Refer to the corresponding section and Table 2-42 for further information.

$$t_{sample} = (2 + STC) \times t_{ADCCLK}$$

EQ 12

STC: Sample Time Control value (0–255)

t_{SAMPLE} is the sample time

Table 2-42 • **STC Bits Function**

Name	Bits	Function
STC	[7:0]	Sample time control

Sample time is computed based on the period of ADCCLK.

The second phase is called the distribution phase. During distribution phase, the ADC computes the equivalent digital value from the value stored in the input capacitor. In this phase, the output signal SAMPLE goes back to '0', indicating the sample is completed; but the BUSY signal remains '1', indicating the ADC is still busy for distribution. The distribution time depends strictly on the number of bits. If the ADC is configured as a 10-bit ADC, then 10 ADCCLK cycles are needed. EQ 13 describes the distribution time.

$$t_{distrib} = N \times t_{ADCCLK}$$

EQ 13

N: Number of bits

The last phase is the post-calibration phase. This is an optional phase. The post-calibration phase takes two ADCCLK cycles. The output BUSY signal will remain '1' until the post-calibration phase is completed. If the post-calibration phase is skipped, then the BUSY signal goes to '0' after distribution phase. As soon as BUSY signal goes to '0', the DATAVALID signal goes to '1', indicating the digital result is available on the RESULT output signals. DATAVAILD will remain '1' until the next ADCSTART is asserted. Actel recommends enabling post-calibration to compensate for drift and temperature-dependent effects. This ensures that the ADC remains consistent over time and with temperature. The post-calibration phase is enabled by bit 3 of the Mode register. EQ 14 describes the post-calibration time.

$$t_{post\text{-}cal} = MODE[3] \times (2 \times t_{ADCCLK})$$

EQ 14

MODE[3]: Bit 3 of the Mode register, described in Table 2-40 on page 2-99.

The calculation for the conversion time for the ADC is summarized in EQ 15.

$$t_{conv} = t_{sync\_read} + t_{sample} + t_{distrib} + t_{post\text{-}cal} + t_{sync\_write}$$

EQ 15

t_{conv}: conversion time

t_{sync_read}: maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, t_{SYSCLK}.

t_{sample}: Sample time

$t_{distrib}$: Distribution time

$t_{post\text{-}cal}$: Post-calibration time

t_{sync_write}: Maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, t_{SYSCLK}.

Example

This example shows how to choose the correct settings to achieve the fastest sample time in 10-bit mode for a system that runs at 66 MHz.

The period of SYSCLK: t_{SYSCLK} = 1/66 MHz = 0.015 µs

Choosing TVC between 1 and 33 will meet the maximum and minimum period for the ADCCLK requirement. A higher TVC leads to a higher ADCCLK period.

The minimum TVC is chosen so that $t_{distrib}$ and $t_{post\text{-}cal}$ can be run faster. The period of ADCCLK with a TVC of 1 can be computed by EQ 16.

$$t_{ADCCLK} = 4 \times (1 + TVC) \times t_{SYSCLK} = 4 \times (1 + 1) \times 0.015\ \mu s = 0.12\ \mu s$$

EQ 16

From Table 2-47 on page 2-117, minimum conversion for 10-bit mode is 1.8 µs. To compute STC, the calculation will first compute the post-calibration time, second the distribution time, and finally the STC setting.

Since Actel recommends post-calibration for temperature drift over time, post-calibration shall be enabled and the post-calibration time, $t_{post\text{-}cal}$, can be computed by EQ 17. The post-calibration time is 0.24 µs.

$$t_{post\text{-}cal} = 2 \times t_{ADCCLK} = 0.24\ \mu s$$

EQ 17

The distribution time, $t_{distrib}$, is equal to 1.2 µs and can be computed using EQ 18.

$$t_{distrib} = N \times t_{ADCCLK} = 10 \times 0.12 = 1.2\ \mu s$$

EQ 18

The STC value can now be computed through EQ 19. The sample time is equal to 0.32 µs. By rearranging EQ 12 on page 2-99 with a t_{sample} of 0.35 µs, the STC can be computed.

$$t_{sample} = t_{conv} - t_{post\text{-}cal} - t_{distrib} - t_{sync\_read} - t_{sync\_write}$$
$$= 1.8\ \mu s - 0.24\ \mu s - 1.2\ \mu s - 0.15\ \mu s - 0.15\ \mu s = 0.32\ \mu s$$

$$STC = \frac{t_{sample}}{t_{ADCCLK}} - 2 = \frac{0.35\ \mu s}{0.12\ \mu s} - 2 = 2.85$$

EQ 19

And so, STC will be rounded up to 3 to ensure the minimum conversion time is met. The sample time, t_{sample}, with an STC of 3, is now equal to 0.36 µs.

The total sample time, using EQ 20, can now be summated.

$$t_{sync\_read} + t_{sample} + t_{distrib} + t_{post\text{-}cal} + t_{sync\_write} = 0.015\ \mu s + 0.36\ \mu s + 1.2\ \mu s + 0.24\ \mu s + 0.015\ \mu s$$
$$= 1.85\ \mu s$$

EQ 20

The optimal setting for the system running at 66 MHz with an ADC for 10-bit mode chosen is listed as follows:

TVC[7:0]	= 1	= 0x01
STC[7:0]	= 3	= 0x03
MODE[3:0]	= b'0100	= 0x4*

*Note that no power-down after every conversion is chosen in this case; however, if the application is power-sensitive, the MODE[2] can be set to '0', as described above, and it will not affect any performance.

Integrated Voltage Reference

The Fusion device has an integrated on-chip 2.56 V reference voltage for the ADC. The value of this reference voltage was chosen to make the prescaling and postscaling factors for the prescaler blocks change in a binary fashion. However, if desired, an external reference voltage of up to 3.3 V can be connected between the VAREF and GNDREF pins. The VAREFSEL control pin is used to select the reference voltage.

Table 2-43 • **VAREF Bit Function**

Name	Bit	Function
VAREF	0	Reference voltage selection 0 – Internal voltage reference selected. VAREF pin outputs 2.56 V. 1 – Input external voltage reference from VAREF and GNDREF

ADC Operation Description

The ADC can be powered down independently of the FPGA core, as an additional control or for power-saving considerations, via the PWRDWN pin of the Analog Block. The PWRDWN pin controls only the comparators in the ADC.

Once the ADC has powered up and been released from reset, ADCRESET, the ADC will initiate a calibration routine designed to provide optimal ADC performance. The Fusion ADC offers a robust calibration scheme to reduce integrated offset and linearity errors. The offset and linearity errors of the main capacitor array are compensated for with an 8-bit calibration capacitor array. The offset/linearity error calibration is carried out in two ways. First, a power-up calibration is carried out when the ADC comes out of reset. This is initiated by the CALIBRATE output of the Analog Block macro and is a fixed number of ADC_CLK cycles (3,840 cycles), as shown in Figure 2-79 on page 2-103. In this mode, the linearity and offset errors of the capacitors are calibrated.

To further compensate for drift and temperature-dependent effects, every conversion is followed by post-calibration of either the offset or a bit of the main capacitor array. The post-calibration ensures that, over time and with temperature, the ADC remains consistent.

After both calibration and the setting of the appropriate configurations, as explained above, the ADC is ready for operation. Setting the ADCSTART signal high for one clock period will initiate the sample and conversion of the analog signal on the channel as configured by CHNUMBER[4:0]. The status signals SAMPLE and BUSY will show when the ADC is sampling and converting (Figure 2-81 on page 2-104). Both SAMPLE and BUSY will initially go high. After the ADC has sampled and held the analog signal, SAMPLE will go low. After the entire operation has completed and the analog signal is converted, BUSY will go low and DATAVALID will go high. This indicates that the digital result is available on the RESULT[11:0] pins.

DATAVALID will remain high until a subsequent ADC_START is issued. The DATAVALID goes low on the rising edge of SYSCLK, as shown in Figure 2-80 on page 2-103. The RESULT signals will be kept constant until the ADC finishes the subsequent sample. The next sampled RESULT will be available when DATAVALID goes high again. It is ideal to read the RESULT when DATAVALID is '1'. The RESULT is latched and remains unchanged until the next DATAVLAID rising edge.

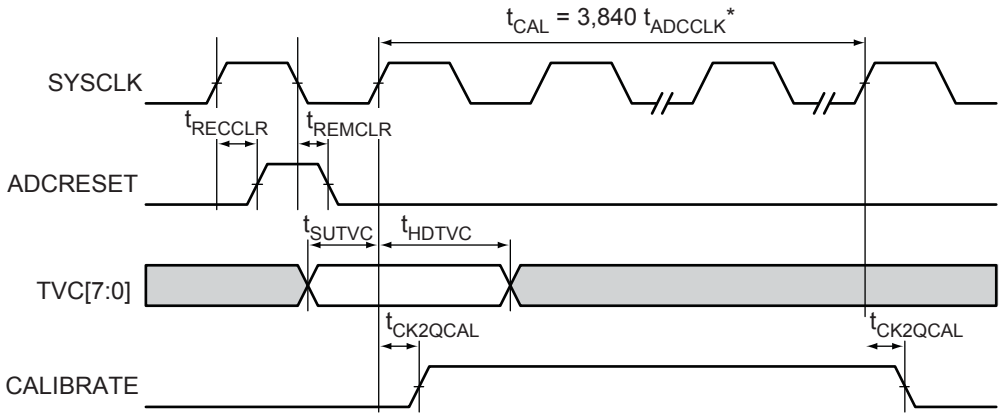
Intra-Conversion

Performing a conversion during power-up, calibration is possible but should be avoided, since the performance is not guaranteed, as shown in Table 2-46 on page 2-114. This is described as intra-conversion. Figure 2-82 on page 2-104 shows intra-conversion (conversion that starts before a conversion is finished).

Injected Conversion

A conversion can be interrupted by another conversion. Before the current conversion is finished, a second conversion can be started by issuing a pulse on signal ADCSTART. When a second conversion is issued before the current conversion is completed, the current conversion would be dropped and the ADC would start the second conversion on the rising edge of the SYSCLK. This is known as injected conversion. Since the ADC is synchronous, the minimum time to issue a second conversion is two clock cycles of SYSCLK after the previous one. Figure 2-83 on page 2-105 shows injected conversion (conversion that starts during the power-up calibration). The total time for calibration still remains 3,840 ADCCLK cycles.

Timing Diagram



*Note: *Refer to EQ 11 on page 2-99 for the calculation on the period of ADCCLK, t_{ADCCLK}.*

Figure 2-79 • **Power-Up Calibration Status Signal Timing Diagram**

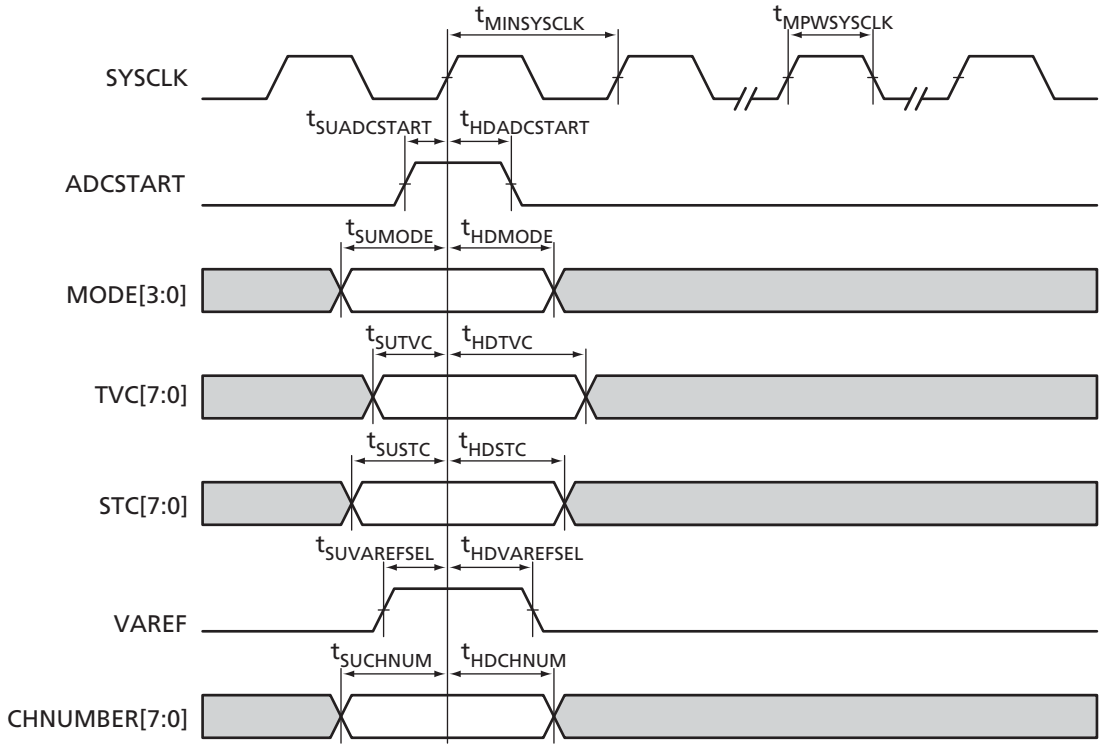
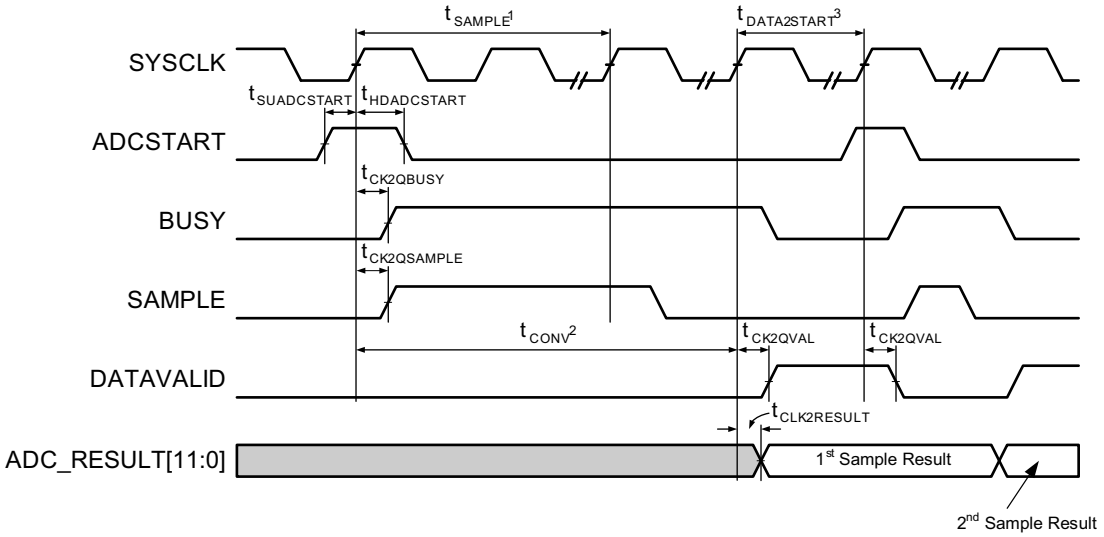


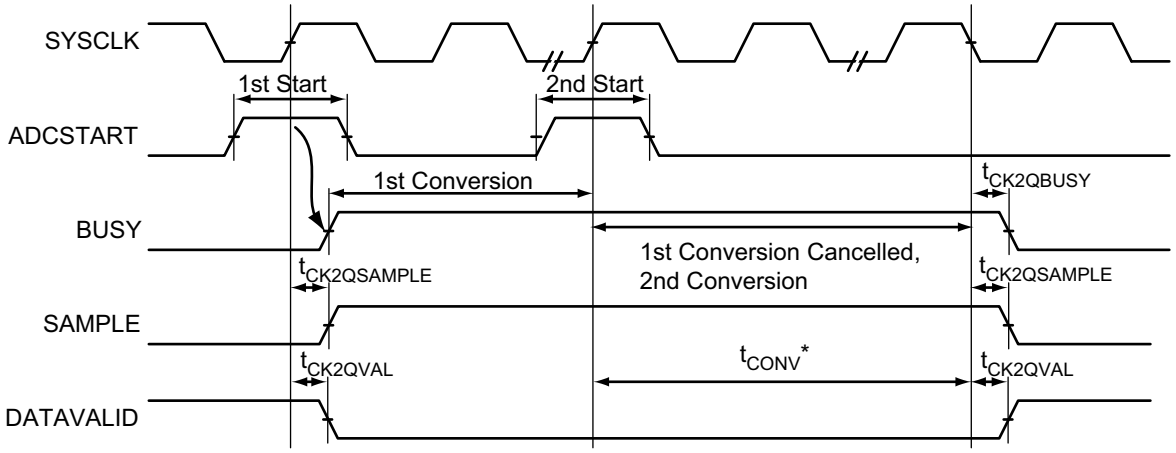
Figure 2-80 • **Input Setup Time**



Notes:

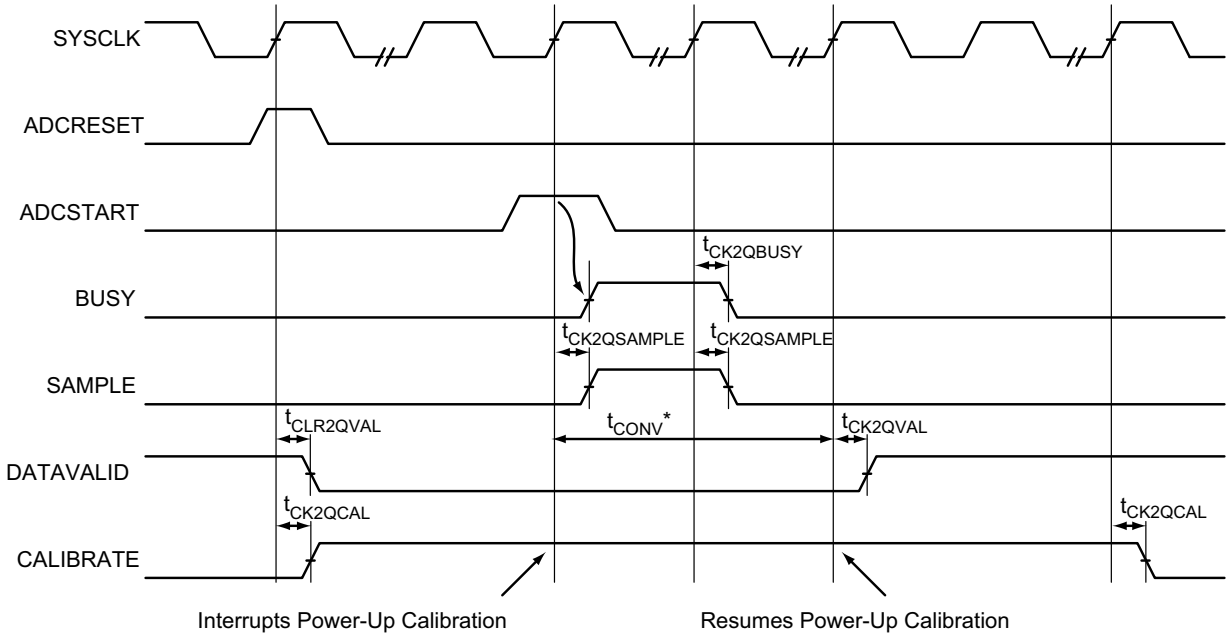
1. *Refer to EQ 12 on page 2-99 for the calculation on the sample time, t_{SAMPLE}.*
2. *See EQ 20 on page 2-101 for calculation on the conversion time, t_{CONV}.*
3. *Minimum time to issue an ADCSTART after DATAVALID is 1 SYSCLK period*

Figure 2-81 • **Standard Conversion Status Signal Timing Diagram**



*Note: *t_{CONV} represents the conversion time of the second conversion. See EQ 10 on page 2-93 for calculation of the conversion time, t_{CONV}.*

Figure 2-82 • **Intra-Conversion Timing Diagram**



*Note: * See EQ 10 on page 2-93 for calculation on the conversion time, t_{CONV}.*

Figure 2-83 • **Injected-Conversion Timing Diagram**

ADC Interface Timing

Table 2-44 • ADC Interface Timing, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{SUMODE}	Mode Pin Setup Time	0.58	0.66	0.78	ns
t_{HDMODE}	Mode Pin Hold Time	0.00	0.00	0.00	ns
t_{SUTVC}	Clock Divide Control (TVC) Setup Time	0.70	0.79	0.93	ns
t_{HDTVC}	Clock Divide Control (TVC) Hold Time	0.00	0.00	0.00	ns
t_{SUSTC}	Sample Time Control (STC) Setup Time	1.62	1.85	2.18	ns
t_{HDSTC}	Sample Time Control (STC) Hold Time	0.00	0.00	0.00	ns
$t_{SUVAREFSEL}$	Voltage Reference Select (VAREFSEL) Setup Time	0.00	0.00	0.00	ns
$t_{HDVAREFSEL}$	Voltage Reference Select (VAREFSEL) Hold Time	0.00	0.00	0.00	ns
$t_{SUCHNUM}$	Channel Select (CHNUMBER) Setup Time	0.93	1.06	1.24	ns
$t_{HDCHNUM}$	Channel Select (CHNUMBER) Hold Time	0.00	0.00	0.00	ns
$t_{SUADCSTART}$	Start of Conversion (ADCSTART) Setup Time	0.77	0.88	1.03	ns
$t_{HDADCSTART}$	Start of Conversion (ADCSTART) Hold Time	0.44	0.50	0.59	ns
$t_{CK2QBUSY}$	Busy Clock-to-Q	1.37	1.56	1.83	ns
$t_{CK2QCAL}$	Power-Up Calibration Clock-to-Q	0.65	0.74	0.86	ns
$t_{CK2QVAL}$	Valid Conversion Result Clock-to-Q	3.21	3.66	4.30	ns
$t_{CK2QSAMPLE}$	Sample Clock-to-Q	0.23	0.26	0.31	ns
$t_{CK2QRESULT}$	Conversion Result Clock-to-Q	2.61	2.98	3.50	ns
$t_{CLR2QBUSY}$	Busy Clear-to-Q	2.12	2.42	2.84	ns
$t_{CLR2QCAL}$	Power-Up Calibration Clear-to-Q	2.22	2.53	2.97	ns
$t_{CLR2QVAL}$	Valid Conversion Result Clear-to-Q	2.48	2.83	3.32	ns
$t_{CLR2QSAMPLE}$	Sample Clear-to-Q	2.24	2.55	3.00	ns
$t_{CLR2QRESULT}$	Conversion result Clear-to-Q	2.32	2.64	3.10	ns
t_{RECCLR}	Recovery Time of Clear	0.00	0.00	0.00	ns
t_{REMCLR}	Removal Time of Clear	0.65	0.74	0.87	ns
$t_{MPWSYSCLK}$	Clock Minimum Pulse Width for the ADC	4.00	4.00	4.00	ns
$t_{FMAXSYSCLK}$	Clock Maximum Frequency for the ADC	10.00	10.00	10.00	MHz

Terminology

Conversion Time

Conversion time is the interval between the release of the hold state (imposed by the input circuitry of a track-and-hold) and the instant at which the voltage on the sampling capacitor settles to within one LSB of a new input value.

DNL – Differential Non-Linearity

For an ideal ADC, the analog-input levels that trigger any two successive output codes should differ by one LSB (DNL = 0). Any deviation from one LSB in defined as DNL (Figure 2-84).

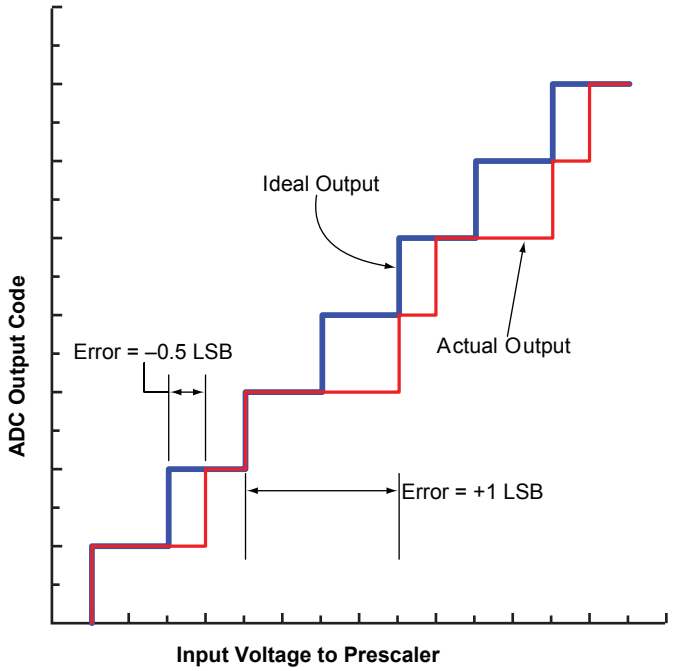


Figure 2-84 • **Differential Non-Linearity (DNL)**

ENOB – Effective Number of Bits

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists only of quantization of noise. As the input frequency increases, the overall noise (particularly in the distortion components) also increases, thereby reducing the ENOB and SINAD (also see the "SINAD – Signal-to-Noise and Distortion" section on page 2-110). ENOB for a full-scale, sinusoidal input waveform is computed using EQ 21.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

EQ 21

FS Error – Full-Scale Error

Full-scale error is the difference between the actual value that triggers that transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error.

Gain Error

The gain error of an ADC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or as a percent of full-scale (%FSR). Gain error is the full-scale error minus the offset error (Figure 2-85).

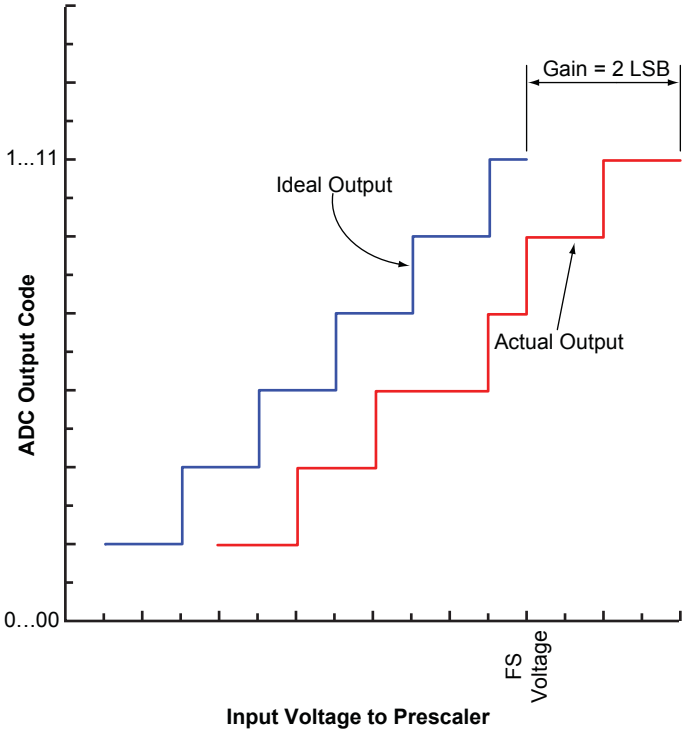


Figure 2-85 • **Gain Error**

Gain Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature, typically expressed in ppm/°C.

INL – Integral Non-Linearity

INL is the deviation of an actual transfer function from a straight line. After nullifying offset and gain errors, the straight line is either a best-fit straight line or a line drawn between the end points of the transfer function (Figure 2-86).

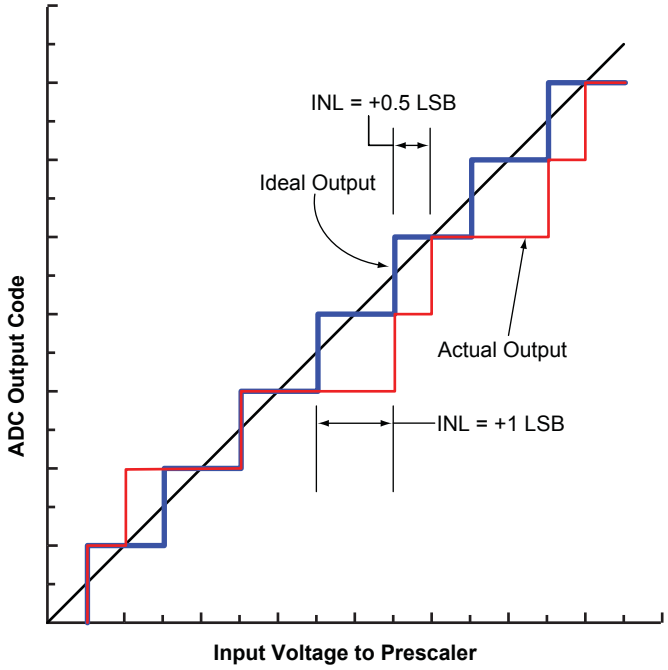


Figure 2-86 • **Integral Non-Linearity (INL)**

LSB – Least Significant Bit

In a binary number, the LSB is the least weighted bit in the group. Typically, the LSB is the furthest right bit. For an ADC, the weight of an LSB equals the full-scale voltage range of the converter divided by 2^N, where N is the converter's resolution.

EQ 22 shows the calculation for a 10-bit ADC with a unipolar full-scale voltage of 2.56 V:

$$1\ \text{LSB} = (2.56\ \text{V} / 2^{10}) = 2.5\ \text{mV}$$

EQ 22

No Missing Codes

An ADC has no missing codes if it produces all possible digital codes in response to a ramp signal applied to the analog input.

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point. For an ideal ADC, the first transition occurs at 0.5 LSB above zero. The offset voltage is measured by applying an analog input such that the ADC outputs all zeroes and increases until the first transition occurs (Figure 2-87).

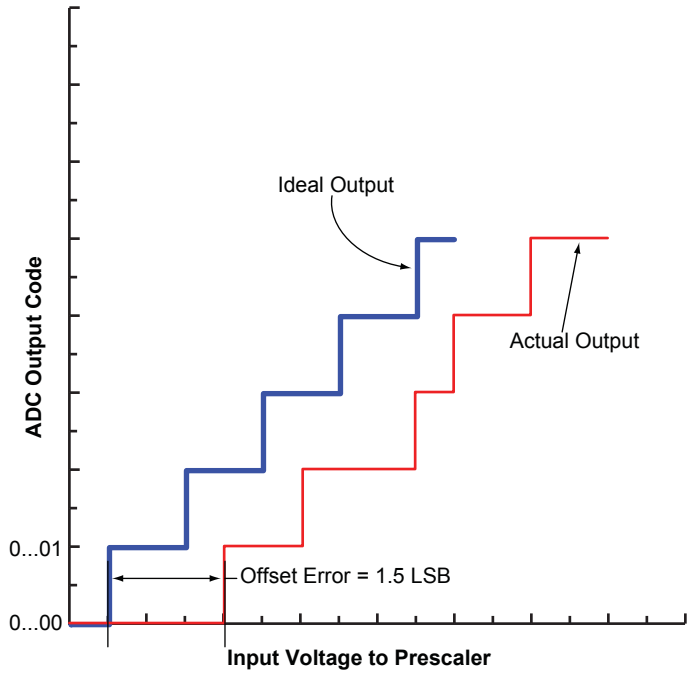


Figure 2-87 • **Offset Error**

Resolution

ADC resolution is the number of bits used to represent an analog input signal. To more accurately replicate the analog signal, resolution needs to be increased.

Sampling Rate

Sampling rate or sample frequency, specified in samples per second (sps), is the rate at which an ADC acquires (samples) the analog input.

SNR – Signal-to-Noise Ratio

SNR is the ratio of the amplitude of the desired signal to the amplitude of the noise signals at a given point in time. For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR (EQ 23) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum ADC noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[MAX]} = 6.02_{dB} \times N + 1.76_{dB}$$

EQ 23

SINAD – Signal-to-Noise and Distortion

SINAD is the ratio of the rms amplitude to the mean value of the root-sum-square of the all other spectral components, including harmonics, but excluding DC. SINAD is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion.

Total Harmonic Distortion

THD measures the distortion content of a signal, and is specified in decibels relative to the carrier (dBc). THD is the ratio of the RMS sum of the selected harmonics of the input signal to the fundamental itself. Only harmonics within the Nyquist limit are included in the measurement.

TUE – Total Unadjusted Error

TUE is a comprehensive specification that includes linearity errors, gain error, and offset error. It is the worst-case deviation from the ideal device performance. TUE is a static specification (Figure 2-88).

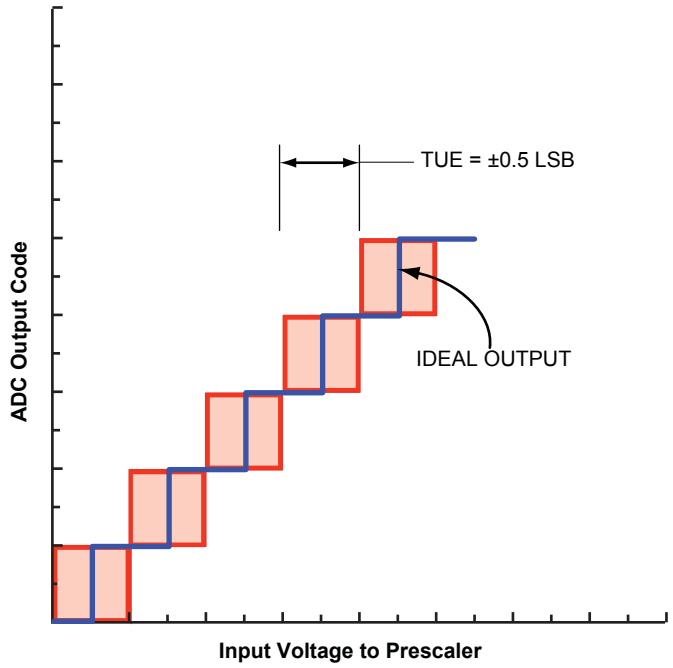


Figure 2-88 • **Total Unadjusted Error (TUE)**

Typical Performance Characteristics

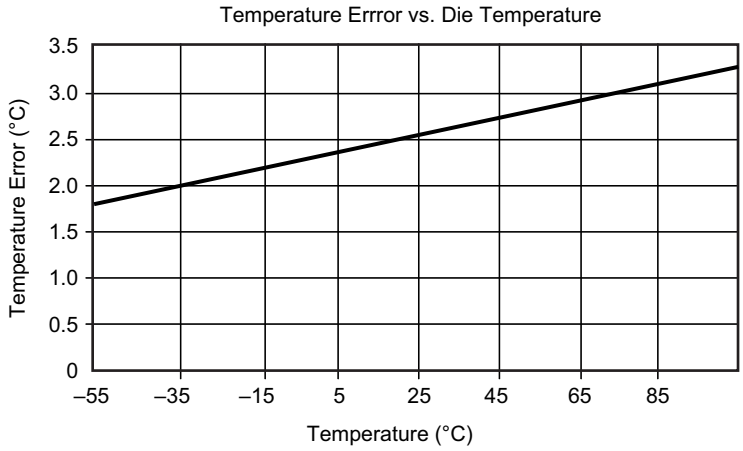


Figure 2-89 • **Temperature Error**

Table 2-45 • **Temperature vs. Average Fitted Error**

Temperature (°C)	Averaged Fitted Error
100	3.2469
90	3.1559
80	3.0649
70	2.9739
60	2.8829
50	2.7919
40	2.7009
30	2.6099
20	2.5189
10	2.4279
0	2.3369
–10	2.2459
–20	2.1549
–30	2.0639
–40	1.9729
–55	1.8364

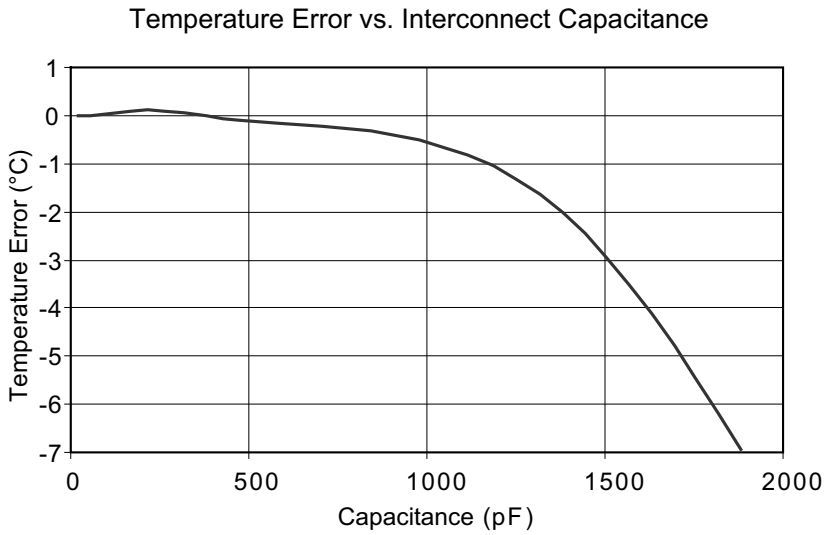


Figure 2-90 • **Effect of External Sensor Capacitance**

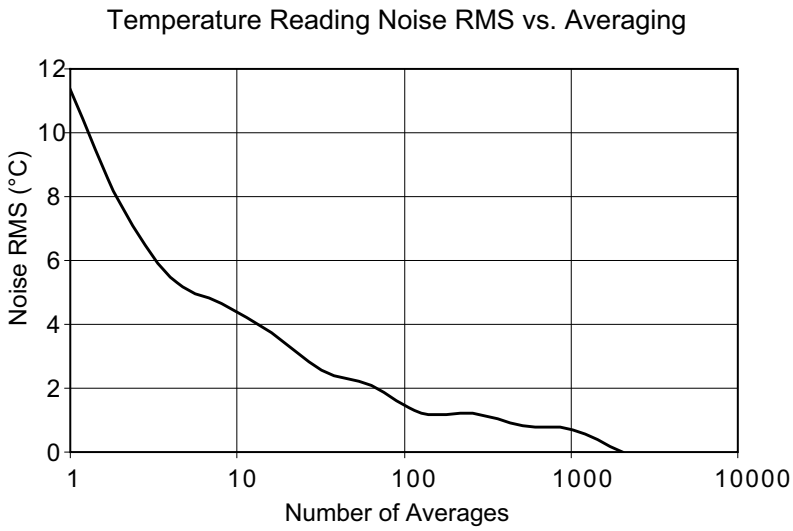


Figure 2-91 • **Temperature Reading Noise When Averaging is Used**

Analog System Characteristics

Table 2-46 • Analog Channel Specifications
Extended Temperature Range Conditions, T_J = 100°C (unless noted otherwise),
Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Voltage Monitor Using Analog Pads AV, AC and AT (using prescaler)						
	Input Voltage (Prescaler)	Refer to Table 3-2 on page 3-3.				
V_{INAP}	Uncalibrated Gain and Offset Errors	Refer to Table 2-48 on page 2-119.				
	Calibrated Gain and Offset Errors	Refer to Table 2-49 on page 2-120.				
	Bandwidth1				100	KHz
	Input Resistance	Refer to Table 3-3 on page 3-5.				
	Scaling Factor	Prescaler modes (Table 2-54 on page 2-128).				
	Sample Time		10			µs
Current Monitor Using Analog Pads AV and AC						
V_{RSM}[1]	Maximum Differential Input Voltage				VAREF / 10	mV
	Resolution	Refer to the "Current Monitor" section.				
	Common Mode Range				–10.5 to +12	V
CMRR	Common Mode Rejection Ratio	DC – 1 KHz	59	60		dB
		1 KHz - 10 KHz	49	50		dB
		> 10 KHz	29	30		dB
t_{CMSHI}	Strobe High time		ADC conv. time		200	µs
t_{CMSHI}	Strobe Low time		5			µs
t_{CMSHI}	Settling time		0.02			µs
	Accuracy	Input differential voltage > 50 mV			–2 – (0.05 x V_{RSM}) to +2 + (0.05 x V_{RSM})	mV

Notes:

1. *V_{RSM} is the maximum voltage drop across the current sense resistor.*
2. *Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as V_{IND} does not exceed these limits.*
3. *V_{IND} is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.*
4. *An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.*
5. *The temperature offset is a fixed positive value.*
6. *The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
7. *When using SmartGen Analog System Builder, CalibIP is required to obtain 0 offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User's Guide.*

Table 2-46 • Analog Channel Specifications (continued)
Extended Temperature Range Conditions, T_J = 100°C (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Temperature Monitor Using Analog Pad AT						
External Temperature Monitor (external diode 2N3904, T_J = 25°C)[4]	Resolution	8-bit ADC		4		°C
		10-bit ADC		1		°C
		12-bit ADC		0.25		°C
	Offset[5]	AFS600, AFS1500 uncalibrated[7]		11		°C
		AFS600, AFS1500 calibrated[7]		0		°C
	Accuracy			±3	±5	°C
	External Sensor Source Current	High level, TMSTBx = 0		10		µA
		Low level, TMSTBx = 1		100		µA
	Max Capacitance on AT pad				1.3	nF
Internal Temperature Monitor	Resolution	8-bit ADC	4			°C
		10-bit ADC	1			°C
		12-bit ADC	0.25			°C
	Offset[5]	AFS600, AFS1500 uncalibrated[7]	11			°C
		AFS600, AFS1500 calibrated[7]	0			°C
	Accuracy			±3	±5	°C
t_{TMSHI}	Strobe High time		10		105	µs
t_{TMSLO}	Strobe Low time		5			µs
t_{TMSSET}	Settling time		5			µs

Notes:

1. *V_{RSM} is the maximum voltage drop across the current sense resistor.*
2. *Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as V_{IND} does not exceed these limits.*
3. *V_{IND} is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.*
4. *An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.*
5. *The temperature offset is a fixed positive value.*
6. *The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
7. *When using SmartGen Analog System Builder, CalibIP is required to obtain 0 offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User's Guide.

Table 2-46 • Analog Channel Specifications (continued)
Extended Temperature Range Conditions, T_J = 100°C (unless noted otherwise),
Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Digital Input using Analog Pads AV, AC and AT						
V_{IND}[2,3]	Input Voltage	Refer to Table 3-2 on page 3-3				
V_{HYSDIN}	Hysteresis			0.3		V
V_{IHDIN}	Input High			1.2		V
V_{ILDIN}	Input Low			0.9		V
V_{MPWDIN}	Minimum Pulse With		50			ns
F_{DIN}	Maximum Frequency				10	MHz
I_{STBDIN}	Input Leakage Current			2		µA
I_{DYNDIN}	Dynamic Current			20		µA
t_{INDIN}	Input Delay			10		ns
Gate Driver Output Using Analog Pad AG						
V_G	Voltage Range	Refer to Table 3-2 on page 3-3				
I_G	Output Current Drive	High Current Mode[6] at 1.0 V			±20	mA
		Low Current Mode: ±1 µA	0.8	1.0	1.3	µA
		Low Current Mode: ±3 µA	2.0	2.7	3.3	µA
		Low Current Mode: ± 10 µA	7.4	9.0	11.5	µA
		Low Current Mode: ± 30 µA	21.0	27.0	32.0	µA
I_{OFFG}	Maximum Off Current				100	nA
F_G	Maximum switching rate	High Current Mode[6] at 1.0 V, 1 kΩ resistive load		1.3		MHz
		Low Current Mode: ±1 µA, 3 MΩ resistive load		3		KHz
		Low Current Mode: ±3 µA, 1 MΩ resistive load		7		KHz
		Low Current Mode: ±10 µA, 300 kΩ resistive load		25		KHz
		Low Current Mode: ±30 µA, 105 kΩ resistive load		78		KHz

Notes:

1. *V_{RSM} is the maximum voltage drop across the current sense resistor.*
2. *Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as V_{IND} does not exceed these limits.*
3. *V_{IND} is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.*
4. *An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.*
5. *The temperature offset is a fixed positive value.*
6. *The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
7. *When using SmartGen Analog System Builder, CalibIP is required to obtain 0 offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User's Guide.

Table 2-47 • **Electrical Characteristics**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
ADC						
VREFADC	Reference voltage	Internal reference		2.560		V
		External reference	2.527		VCC33A + 0.05	V
t_{CONV}	Conversion time	8-bit mode	1.67			µs
		10-bit mode	1.82			µs
		12-bit mode	2.00			µs
	Sample rate1	8-bit mode			600	ksps
		10-bit mode			550	ksps
		12-bit mode			500	ksps
All Analog Inputs (direct input)						
VINAD	Input voltage		–0.2		≤ VREF	V
CINAD	Input capacitance	Channel not selected		7		pF
		Channel selected, not sampling		8		pF
		Channel selected and sampling		18		pF
TUE	Total unadjusted error (external reference)	10-bit mode Input impedance 2 kΩ		2		LSB
All Analog Inputs (using prescaler)						
VINAP	Input voltage[2]		–12		12	V
	Accuracy	Positive DC inputs		1		%
		Negative DC inputs		2		%
	Offset			2 ± 0.2% of range		mV
	Bandwidth		100			kHz
	Impedance (2, 4, 8, and 12 V ranges)		1			MΩ
	Scaling factor	Pre-Scaler Modes (Table 2-35 on page 2-80)				
	Settling time	To 0.1% of final value			10	µs
Current Monitor						
VRSM	Maximum Differential Input				VREFADC/10	mV
	Resolution		1			mV
	Common Mode Range		–12		12	V
	Gain			10		
CMRR	Common mode rejection ratio	DC – 1 kHz		60		dB
		1 kHz – 10 kHz		50		dB
		> 10 kHz		30		dB
	Pole			100		kHz
VMPWC	Strobe	Minimum Pulse Width	10			µs

Notes:

1. *The sample rate is time-shared among active analog inputs.*
2. *The input voltage range for the temperature monitor block prescaler is 0 to 12 V.*
3. *VRSM is the maximum voltage drop across the current sense resistor.*

Table 2-47 • **Electrical Characteristics (continued)**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Temperature Monitor						
	Resolution			1		ºC
	Accuracy			5	± 10	ºC
VMPWT	Strobe	Minimum Pulse Width	10			µs
Analog Input as a Digital Input						
VIND	Input voltage		–0.2		AVDD + 0.2	V
VHYSDIN	Hysteresis			0.3		V
VIHDIN	Input High			1.2		V
VILDIN	Input Low			0.9		V
VMPWDIN	Minimum pulse width		100			nS
I_{STBDIN}	Standby current				20	nA
I_{DYNDIN}	Dynamic current				20	µA
t_{INDIN}	Input delay			10		nS
Analog Output Pad (G pad)						
VG	Voltage Range		–12		12	V
IG	Minimum output current drive	High current mode at 1.0 V		25		mA
		Low current mode—1 µA		1		µA
		Low current mode—3 µA		3		µA
		Low current mode—10 µA		10		µA
		Low current mode—30 µA		30		µA
IOFFG	Maximum Off Current			100		µA

Notes:

1. *The sample rate is time-shared among active analog inputs.*
2. *The input voltage range for the temperature monitor block prescaler is 0 to 12 V.*
3. *VRSM is the maximum voltage drop across the current sense resistor.*

Table 2-48* • Uncalibrated Analog Channel Accuracy
Worst-Case Extended Temperature Conditions, T_J = 100°C

		Total Channel Error (LSB)			Channel Input Offset Error (LSB)			Channel Input Offset Error (mV)			Channel Gain Error (%FSR)		
Analog Pad	**Prescaler Range (V)**	**Neg. Max.**	**Med.**	**Pos. Max.**	**Neg Max**	**Med.**	**Pos. Max.**	**Neg. Max.**	**Med.**	**Pos. Max.**	**Min.**	**Typ.**	**Max.**
Positive Range		**ADC in 10-Bit Mode**											
AV, AC	16	–22	–2	12	–11	–2	14	–169	–32	224	3	0	–3
	8	–40	–5	17	–11	–5	21	–87	–40	166	2	0	–4
	4	–45	–9	24	–16	–11	36	–63	–43	144	2	0	–4
	2	–70	–19	33	–33	–20	66	–66	–39	131	2	0	–4
	1	–25	–7	5	–11	–3	26	–11	–3	26	3	–1	–3
	0.5	–41	–12	8	–12	–7	38	–6	–4	19	3	–1	–3
	0.25	–53	–14	19	–20	–14	40	–5	–3	10	5	0	–4
	0.125	–89	–29	24	–40	–28	88	–5	–4	11	7	0	–5
AT	16	–3	9	15	–4	0	4	–64	5	64	1	0	–1
	4	–10	2	15	–11	–2	11	–44	–8	44	1	0	–1
Negative Range		**ADC in 10-Bit Mode**											
AV, AC	16	–35	–10	9	–24	–6	9	–383	–96	148	5	–1	–6
	8	–65	–19	12	–34	–12	9	–268	–99	75	5	–1	–5
	4	–86	–28	21	–64	–24	19	–254	–96	76	5	–1	–6
	2	–136	–53	37	–115	–42	39	–230	–83	78	6	–2	–7
	1	–98	–35	8	–39	–8	15	–39	–8	15	10	–3	–10
	0.5	–121	–46	7	–54	–14	18	–27	–7	9	10	–4	–11
	0.25	–149	–49	19	–72	–16	40	–18	–4	10	14	–4	–12
	0.125	–188	–67	38	–112	–27	56	–14	–3	7	16	–5	–14

*Note: *Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Gain remains the same.*

Table 2-49 • Calibrated Analog Channel Accuracy [1,2,3]
Worst-Case Extended Temperature Conditions, T_J = 100°C

		Condition	Total Channel Error (LSB)		
Analog Pad	**Prescaler Range (V)**	**Input Voltage[4] (V)**	**Negative Max.**	**Median**	**Positive Max.**
Positive Range			**ADC in 10-Bit Mode**		
AV, AC	16	0.300 to 12.0	–6	1	6
	8	0.250 to 8.00	–6	0	6
	4	0.200 to 4.00	–7	–1	7
	2	0.150 to 2.00	–7	0	7
	1	0.050 to 1.00	–6	–1	6
AT	16	0.300 to 16.0	–5	0	5
	4	0.100 to 4.00	–7	–1	7
Negative Range			**ADC in 10-Bit Mode**		
AV, AC	16	–0.400 to –10.5	–7	1	9
	8	–0.350 to –8.00	–7	–1	7
	4	–0.300 to –4.00	–7	–2	9
	2	–0.250 to –2.00	–7	–2	7
	1	–0.050 to –1.00	–16	–1	20

Notes:

1. *Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Overall accuracy remains the same.*
2. *Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User's Guide*.*
3. *Calibrated with two-point calibration methodology, using 20% and 80% full-scale points.*
4. *The lower limit of the input voltage is determined by the prescaler input offset.*

Table 2-50 • Analog Channel Accuracy: Monitoring Standard Positive Voltages Typical Conditions, T_A = 25°C

Input Voltage (V)	Calibrated Typical Error per Positive Prescaler Setting [1] (%FSR)							Direct ADC [2,3] (%FSR)
	16 V (AT)	16 V (12 V) (AV/AC)	8 V (AV/AC)	4 V (AT)	4 V (AV/AC)	2 V (AV/AC)	1 V (AV/AC)	VAREF = 2.56 V
15	1							
14	1							
12	1	1						
5	2	2	1					
3.3	2	2	1	1	1			
2.5	3	2	1	1	1			1
1.8	4	4	1	1	1	1		1
1.5	5	5	2	2	2	1		1
1.2	7	6	2	2	2	1		1
0.9	9	9	4	3	3	1	1	1

Notes:

1. *Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User's Guide*.*
2. *Direct ADC mode using an external VAREF of 2.56V±4.6mV, without Analog Calibration macro.*
3. *For input greater than 2.56 V, the ADC output will saturate. A higher VAREF or prescaler usage is recommended.*

Examples

Calculating Accuracy for an Uncalibrated Analog Channel

Formula

For a given prescaler range, EQ 24 gives the output voltage.

$$\text{Output Voltage} = (\text{Channel Output Offset in V}) + (\text{Input Voltage} \times \text{Channel Gain}) \quad \text{EQ 24}$$

where

Channel Output offset in V = Channel Output offset in LSBs x Equivalent voltage per LSB

Channel Gain Factor = 1+ (% Channel Gain / 100)

Example

Input Voltage = 5 V

Chosen Prescaler range = 8 V range

Refer to Table 2-48 on page 2-119.

Max. Output Voltage = (Max Positive output offset) + (Input Voltage x Max Gain Factor)

Max. Positive output offset = (8 LSB) x (8mV per LSB in 10-bit mode)

Max. Positive output offset = 64 mV

Max. Gain = 1 + (2/100)

Max. Gain = 1.02

Max. Output Voltage = (64 mV) + (5 V x 1.02)

Max. Output Voltage = **5.164 V**

Similarly,

Min. Output Voltage = (Min. Negative output offset) + (Input Voltage x Min. Gain)

= (–136 mV) + (5 V x 0.98) = **4.764 V**

Calculating Accuracy for a Calibrated Analog Channel

Formula

For a given prescaler range, EQ 25 gives the output voltage.

$$\text{Output Voltage} = \text{Channel TUE in V} + \text{Input Voltage} \quad \text{EQ 25}$$

where

Channel TUE in V = Channel TUE in LSBs x Equivalent voltage per LSB

Example

Input Voltage = 5 V

Chosen Prescaler range = 8 V range

Refer to Table 2-49 on page 2-120.

Max. Output Voltage = Max. Channel TUE in V + Input Voltage

Max. Channel TUE in V = (6 LSB) × (8 mV per LSB in 10-bit mode) = 48 mV

Max. Output Voltage = 48 mV + 5 V = **5.048 V**

Similarly,

Min Output Voltage = Min Channel TUE in V + Input Voltage = (-48 mV) + 5 V = **4.952 V**

Calculating LSBs from a Given Error Budget

Formula

For a given prescaler range,

LSB count = ± (Input Voltage × Required % error) / (Equivalent voltage per LSB)

Example

Input Voltage = 5 V

Required error margin= 1%

Refer to Table 2-49 on page 2-120.

Equivalent voltage per LSB = 16 mV for a 16V prescaler, with ADC in 10-bit mode

LSB Count = ± (5.0 V × 1%) / (0.016)

LSB Count = **± 3.125**

Equivalent voltage per LSB = **8 mV** for an 8 V prescaler, with ADC in 10-bit mode

LSB Count = ± (5.0 V × 1%) / (0.008)

LSB Count = **± 6.25**

The 8 V prescaler satisfies the calculated LSB count accuracy requirement (see Table 2-49 on page 2-120).

Analog Configuration MUX

The ACM is the interface between the FPGA, the Analog Block configurations, and the real-time counter. Actel Libero IDE will generate IP that will load and configure the Analog Block via the ACM. However, users are not limited to using the Libero IDE IP. This section provides a detailed description of the ACM's register map, truth tables for proper configuration of the Analog Block and RTC, as well as timing waveforms so users can access and control the ACM directly from their designs.

The Analog Block contains four 8-bit latches per Analog Quad that are initialized through the ACM. These latches act as configuration bits for Analog Quads. The ACM block runs from the core voltage supply (1.5 V).

Access to the ACM is achieved via 8-bit address and data busses with enables. The pin list is provided in Table 2-35 on page 2-77. The ACM clock speed is limited to a maximum of 10 MHz, more than sufficient to handle the low-bandwidth requirements of configuring the Analog Block and the RTC (sub-block of the Analog Block).

Table 2-51 decodes the ACM address space and maps it to the corresponding Analog Quad and configuration byte for that quad.

Table 2-51 • **ACM Address Decode Table for Analog Quad**

ACMADDR [7:0] in Decimal	Name	Description	Associated Peripheral
0	–	–	Analog Quad
1	AQ0	Byte 0	Analog Quad
2	AQ0	Byte 1	Analog Quad
3	AQ0	Byte 2	Analog Quad
4	AQ0	Byte 3	Analog Quad
5	AQ1	Byte 0	Analog Quad
⋮	⋮	⋮	Analog Quad
36	AQ8	Byte 3	Analog Quad
37	AQ9	Byte 0	Analog Quad
38	AQ9	Byte 1	Analog Quad
39	AQ9	Byte 2	Analog Quad
40	AQ9	Byte 3	Analog Quad
41		Undefined	Analog Quad
⋮	⋮	Undefined	Analog Quad
63		Undefined	RTC
64	COUNTER0	Counter bits 7:0	RTC
65	COUNTER1	Counter bits 15:8	RTC
66	COUNTER2	Counter bits 23:16	RTC
67	COUNTER3	Counter bits 31:24	RTC
68	COUNTER4	Counter bits 39:32	RTC
72	MATCHREG0	Match register bits 7:0	RTC
73	MATCHREG1	Match register bits 15:8	RTC
74	MATCHREG2	Match register bits 23:16	RTC
75	MATCHREG3	Match register bits 31:24	RTC
76	MATCHREG4	Match register bits 39:32	RTC
80	MATCHBITS0	Individual match bits 7:0	RTC

Table 2-51 • ACM Address Decode Table for Analog Quad (continued)

ACMADDR [7:0] in Decimal	Name	Description	Associated Peripheral
81	MATCHBITS1	Individual match bits 15:8	RTC
82	MATCHBITS2	Individual match bits 23:16	RTC
83	MATCHBITS3	Individual match bits 31:24	RTC
84	MATCHBITS4	Individual match bits 39:32	RTC
88	CTRL_STAT	Control (write) / Status (read) register bits 7:0	RTC

Note: ACMADDR bytes 1 to 40 pertain to the Analog Quads; bytes 64 to 89 pertain to the RTC.

ACM Characteristics[1]

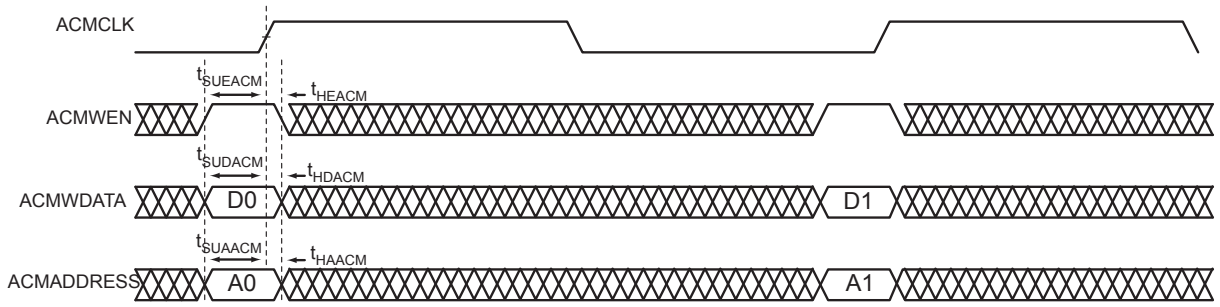


Figure 2-92 • ACM Write Waveform

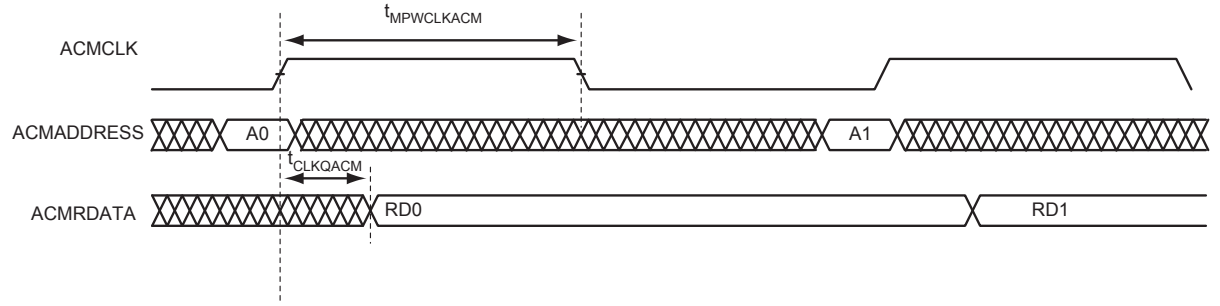


Figure 2-93 • ACM Read Waveform

1. *When addressing the RTC addresses (i.e., ACMADDR 64 to 89), there is no timing generator, and the rc_osc, byte_en, and aq_wen signals have no impact.*

Timing Characteristics

Table 2-52 • Analog Configuration Multiplexer (ACM) Timing, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{CLKQACM}$	Clock-to-Q of the ACM	20.35	23.18	27.25	ns
t_{SUDACM}	Data Setup time for the ACM	4.52	5.15	6.06	ns
t_{HDACM}	Data Hold time for the ACM	0.00	0.00	0.00	ns
t_{SUAACM}	Address Setup time for the ACM	4.87	5.55	6.53	ns
t_{HAACM}	Address Hold time for the ACM	0.00	0.00	0.00	ns
t_{SUEACM}	Enable Setup time for the ACM	4.06	4.62	5.43	ns
t_{HEACM}	Enable Hold time for the ACM	0.00	0.00	0.00	ns
$t_{MPWARACM}$	Asynchronous Reset Minimum Pulse Width for the ACM	10.00	10.00	10.00	ns
$t_{REMARACM}$	Asynchronous Reset Removal time for the ACM	13.39	15.25	17.93	ns
$t_{RECARACM}$	Asynchronous Reset Recovery time for the ACM	13.39	15.25	17.93	ns
$t_{MPWCLKACM}$	Clock Minimum Pulse Width for the ACM	45.00	45.00	45.00	ns
$t_{FMAXCLKACM}$	Clock Maximum Frequency for the ACM	100.00	100.00	100.00	MHz

Analog Quad ACM Description

Table 2-53 maps out the ACM space associated with configuration of the Analog Quads within the Analog Block. Table 2-53 shows the byte assignment within each quad and the function of each bit within each byte. Subsequent tables will explain each bit setting and how it corresponds to a particular configuration. After 3.3 V and 1.5 V are applied to Fusion, Analog Quad configuration registers are loaded with default settings until the initialization and configuration state machine changes them to user-defined settings.

Table 2-53 • **Analog Quad ACM Byte Assignment**

Byte	Bit	Signal (Bx)	Function	Default Setting
Byte 0 (AV)	0	B0[0]	Scaling factor control – prescaler	Highest voltage range
	1	B0[1]		
	2	B0[2]		
	3	B0[3]	Analog MUX select	Prescaler
	4	B0[4]	Current monitor switch	Off
	5	B0[5]	Direct analog input switch	Off
	6	B0[6]	Selects V-pad polarity	Positive
	7	B0[7]	Prescaler op amp mode	Power-down
Byte 1 (AC)	0	B1[0]	Scaling factor control – prescaler	Highest voltage range
	1	B1[1]		
	2	B1[2]		
	3	B1[3]	Analog MUX select	Prescaler
	4	B1[4]		
	5	B1[5]	Direct analog input switch	Off
	6	B1[6]	Selects C-pad polarity	Positive
	7	B1[7]	Prescaler op amp mode	Power-down
Byte 2 (AG)	0	B2[0]	Internal chip temperature monitor	Off
	1	B2[1]	Spare	–
	2	B2[2]	Current drive control	Lowest current
	3	B2[3]		
	4	B2[4]	Spare	–
	5	B2[5]	Spare	–
	6	B2[6]	Selects G-pad polarity	Positive
	7	B2[7]	Selects low/high drive	Low drive
Byte 3 (AT)	0	B3[0]	Scaling factor control – prescaler	Highest voltage range
	1	B3[1]		
	2	B3[2]		
	3	B3[3]	Analog MUX select	Prescaler
	4	B3[4]		
	5	B3[5]	Direct analog input switch	Off
	6	B3[6]	–	–
	7	B3[7]	Prescaler op amp mode	Power-down

Table 2-54 details the settings available to control the prescaler values of the AV, AC, and AT pins. Note that the AT pin has a reduced number of available prescaler values.

Table 2-54 • **Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[2:0]	Scaling Factor, Pad to ADC Input	LSB for an 8-Bit Conversion (mV)	LSB for a 10-Bit Conversion (mV)	LSB for a 12-Bit Conversion (mV)	Full-Scale Voltage	Range Name
000*	0.15625	64	16	4	16.368 V	16 V
001	0.3125	32	8	2	8.184 V	8 V
010*	0.625	16	4	1	4.092 V	4 V
011	1.25	8	2	0.5	2.046 V	2 V
100	2.5	4	1	0.25	1.023 V	1 V
101	5.0	2	0.5	0.125	0.5115 V	0.5 V
110	10.0	1	0.25	0.0625	0.25575 V	0.25 V
111	20.0	0.5	0.125	0.03125	0.127875 V	0.125 V

*Note: *These are the only valid ranges for the temperature monitor block prescaler.*

Table 2-55 details the settings available to control the MUX within each of the AV, AC, and AT circuits. This MUX determines whether the signal routed to the ADC is the direct analog input, prescaled signal, or output of either the Current Monitor Block or the Temperature Monitor Block.

Table 2-55 • **Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[4]	Control Lines Bx[3]	ADC Connected To
0	0	Prescaler
0	1	Direct input
1	0	Current amplifier* temperature monitor
1	1	Not valid

*Note: *Current monitor is not supported between –40°C and –55°C.*

Table 2-56 details the settings available to control the Direct Analog Input switch for the AV, AC, and AT pins.

Table 2-56 • **Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[5]	Direct Input Switch
0	Off
1	On

Table 2-57 details the settings available to control the polarity of the signals coming to the AV, AC, and AT pins. Note that the only valid setting for the AT pin is logic 0 to support positive voltages.

Table 2-57 • **Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)***

Control Lines Bx[6]	Input Signal Polarity
0 [1]	Positive
1 [2]	Negative

Notes:

1. *The B3[6] signal for the AT pad should be kept at logic 0 to accept only positive voltages.*
2. *Negative input is not supported between –40°C and –55°C.*

Table 2-58 details the settings available to either power down or enable the prescaler associated with the analog inputs AV, AC, and AT.

Table 2-58 • **Prescaler Op Amp Power-Down Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[7]	Prescaler Op Amp
0	Power-down
1	Operational

Table 2-59 details the settings available to enable the Current Monitor Block associated with the AC pin.

Table 2-59 • **Current Monitor Input Switch Control Truth Table—AV (x = 0)**

Control Lines B0[4]	Current Monitor Input Switch
0	Off
1 *	On

Note: Current monitor is not supported between –40°C and –55°C.

Table 2-60 details the settings available to configure the drive strength of the gate drive when not in high-drive mode.

Table 2-60 • **Low-Drive Gate Driver Current Truth Table (AG)**

Control Lines B2[3]	Control Lines B2[2]	Current (µA)
0	0	1
0	1	3
1	0	10
1	1	30

Table 2-61 details the settings available to set the polarity of the gate driver (either p-channel- or n-channel-type devices).

Table 2-61 • **Gate Driver Polarity Truth Table (AG)**

Control Lines B2[6]	Gate Driver Polarity
0	Positive
1	Negative

Table 2-62 details the settings available to turn on the Gate Driver and set whether high-drive mode is on or off.

Table 2-62 • **Gate Driver Control Truth Table (AG)**

Control Lines B2[7]	GDON	Gate Driver
0	0	Off
0	1	Low drive on
1	0	Off
1	1	High drive on

Table 2-63 details the settings available to turn on and off the chip internal temperature monitor.

Table 2-63 • **Internal Temperature Monitor Control Truth Table**

Control Lines B2[0]	PDTMB	Chip Internal Temperature Monitor
0	0	Off
1	1	On

User I/Os

Introduction

Fusion devices feature a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. Table 2-65, Table 2-66, Table 2-67, and Table 2-68 on page 2-133 show the voltages and the compatible I/O standards. I/Os provide programmable slew rates, drive strengths, weak pull-up, and weak pull-down circuits. 3.3 V PCI and 3.3 V PCI-X are 5 V–tolerant. See the "5 V Input Tolerance" section on page 2-142 for possible implementations of 5 V tolerance.

All I/Os are in a known state during power-up, and any power-up sequence is allowed without current impact. Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset" section on page 3-6 for more information. In low power standby or sleep mode (V_{CC} is OFF, V_{CC33A} is ON, V_{CCI} is ON) or when the resource is not used, digital inputs are tristated, digital outputs are tristated, and digital bibufs (input/output) are tristated.

I/O Tile

The Fusion I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile in selected I/O banks can be used to support high-performance register inputs and outputs, with register enable if desired (Figure 2-94 on page 2-131). The registers can also be used to support the JESD-79C DDR standard within the I/O structure (see the "Double Data Rate (DDR) Support" section on page 2-137 for more information).

As depicted in Figure 2-95 on page 2-136, all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the "I/O Registers" section on page 2-136 for more information.

I/O Banks and I/O Standards Compatibility

The digital I/Os are grouped into I/O voltage banks. There are four digital I/O banks on the AFS600 and AFS1500 devices. Figure 2-108 on page 2-156 shows the bank configuration. The north side of the I/O in the AFS600 and AFS1500 devices comprises two banks of Actel Pro I/Os. The Actel Pro I/Os support a wide number of voltage-referenced I/O standards in addition to the multitude of single-ended and differential I/O standards common throughout all Actel digital I/Os. Each I/O voltage bank has dedicated I/O supply and ground voltages (VCCI/GNDQ for input buffers and V_{CCI}/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. Table 2-66 and Table 2-67 on page 2-132 show the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks, refer to the specific pin table of the device in the "Pin Assignments" section on page 4-1 and the "User I/O Naming Convention" section on page 2-156.

Each Pro I/O bank is divided into minibanks. Any user I/O in a VREF minibank (a minibank is the region of scope of a VREF pin) can be configured as a VREF pin (Figure 2-94 on page 2-131). Only one VREF pin is needed to control the entire VREF minibank. The location and scope of the VREF minibanks can be determined by the I/O name. For details, see the "User I/O Naming Convention" section on page 2-156.

Table 2-67 on page 2-132 shows the I/O standards supported by Fusion devices and the corresponding voltage levels.

I/O standards are compatible if the following are true:

- Their VCCI values are identical.
- If both of the standards need a VREF, their VREF values must be identical (Pro I/O only).

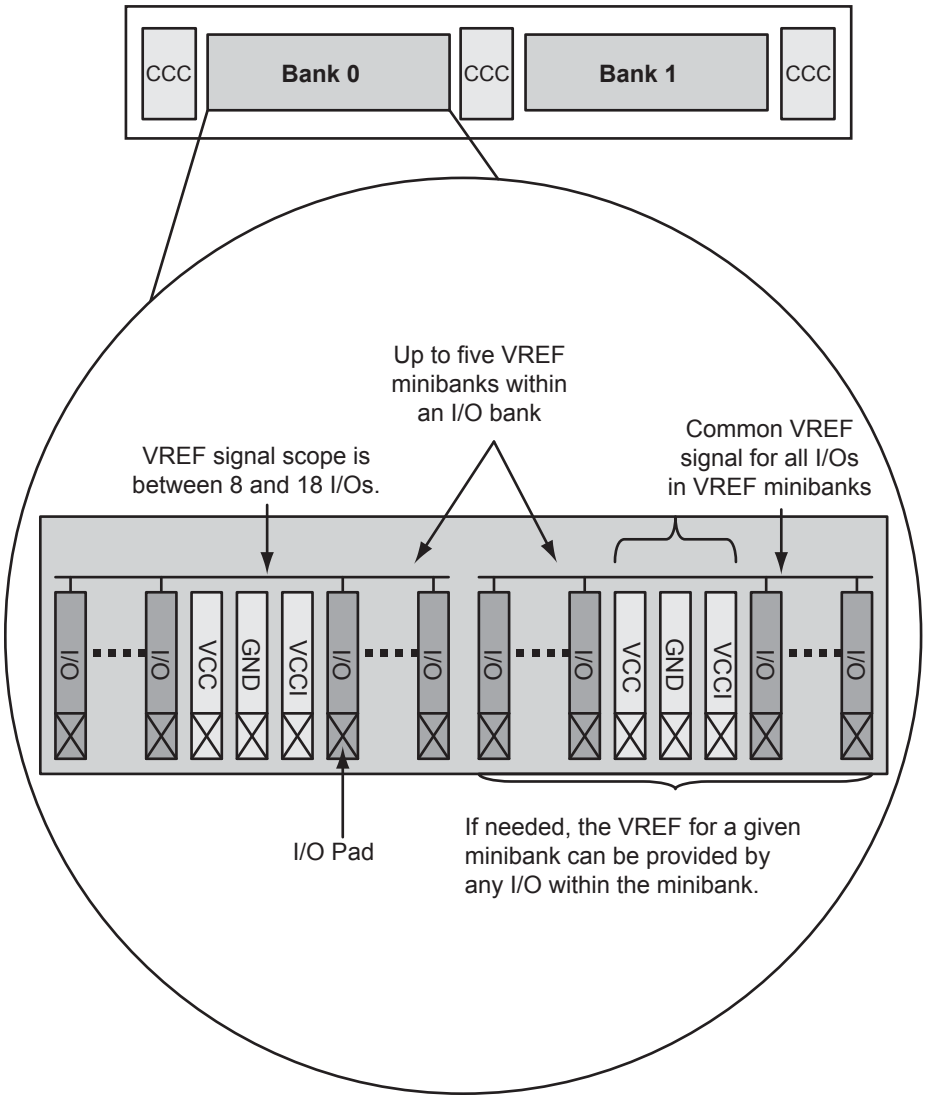


Figure 2-94 • **Fusion Pro I/O Bank Detail Showing VREF Minibanks (north side ofAFS600 and AFS1500)**

Table 2-64 • **I/O Standards Supported by Bank Type**

I/O Bank	Single-Ended I/O Standards	Differential I/O Standards	Voltage-Referenced	Hot-Swap
Advanced I/O	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X	LVPECL and LVDS	–	–
Pro I/O	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X	LVPECL and LVDS	GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II	Yes

Table 2-65 • **I/O Bank Support by Device**

I/O Bank	AFS600	AFS1500
Advanced I/O	E, W	E, W
Pro I/O	N	N
Analog Quad	S	S

Note: E = East side of the device
W = West side of the device
N = North side of the device
S = South side of the device

Table 2-66 • **Fusion VCCI Voltages and Compatible Standards**

VCCI (typical)	Compatible Standards
3.3 V	LVTTL/LVCMOS 3.3, PCI 3.3, SSTL3 (Class I and II),* GTL+ 3.3, GTL 3.3,* LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, SSTL2 (Class I and II),* GTL+ 2.5,* GTL 2.5,* LVDS, B-LVDS, M-LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5, HSTL (Class I),* HSTL (Class II)*

*Note: *I/O standard supported by Pro I/O banks.*

Table 2-67 • **Fusion VREF Voltages and Compatible Standards***

VREF (typical)	Compatible Standards
1.5 V	SSTL3 (Class I and II)
1.25 V	SSTL2 (Class I and II)
1.0 V	GTL+ 2.5, GTL+ 3.3
0.8 V	GTL 2.5, GTL 3.3
0.75 V	HSTL (Class I), HSTL (Class II)

*Note: *I/O standards supported by Pro I/O banks.*

Table 2-68 • **Fusion Advanced I/O Features**

I/O Bank Voltage (typical)	Minibank Voltage (typical)	LVTTL/LVCMOS 3.3 V	LVCMOS 2.5 V	LVCMOS 1.8 V	LVCMOS 1.5 V	3.3 V PCI / PCI-X	GTL + (3.3 V)	GTL + (2.5 V)	GTL (3.3 V)	GTL (2.5 V)	HSTL Class I and II (1.5 V)	SSTL2 Class I and II (2.5 V)	SSTL3 Class I and II (3.3 V)	LVDS (2.5 V ± 5%)	LVPECL (3.3 V)
3.3 V	–														
	0.80 V														
	1.00 V														
	1.50 V														
2.5 V	–														
	0.80 V														
	1.00 V														
	1.25 V														
1.8 V	–														
1.5 V	–														
	0.75 V														

Note: White box: Allowable I/O standard combinations
Gray box: Illegal I/O standard combinations

Features Supported on Pro I/Os

Table 2-69 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

Table 2-69 • **Fusion Pro I/O Features**

Feature	Description
Single-ended and voltage-referenced transmitter features	• Hot insertion in every mode except PCI or 5 V input tolerant (these modes use clamp diodes and do not allow hot insertion) • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os. • Weak pull-up and pull-down • Two slew rates • Skew between output buffer enable/disable time: 2 ns delay (rising edge) and 0 ns delay (falling edge); see "Selectable Skew between Output Buffer Enable/Disable Time" on page 2-147 for more information • Five drive strengths • 5 V–tolerant receiver ("5 V Input Tolerance" section on page 2-142) • LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Output Tolerance" section on page 2-146) • High performance (Table 2-74 on page 2-141)
Single-ended receiver features	• Schmitt trigger option • ESD protection • Programmable delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V) • High performance (Table 2-74 on page 2-141) • Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry
Voltage-referenced differential receiver features	• Programmable Delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V) • High performance (Table 2-74 on page 2-141) • Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry
CMOS-style LVDS, B-LVDS, M-LVDS, or LVPECL transmitter	• Two I/Os and external resistors are used to provide a CMOS-style LVDS, B-LVDS, M-LVDS, or LVPECL transmitter solution. • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os. • Weak pull-up and pull-down • Fast slew rate
LVDS/LVPECL differential receiver features	• ESD protection • High performance (Table 2-74 on page 2-141) • Programmable delay: 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V) • Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry

Table 2-70 • Maximum I/O Frequency for Single-Ended, Voltage-Referenced, and Differential I/Os; All I/O Bank Types (maximum drive strength and high slew selected)

Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	200 MHz
LVCMOS 2.5 V	250 MHz
LVCMOS 1.8 V	200 MHz
LVCMOS 1.5 V	130 MHz
PCI	200 MHz
PCI-X	200 MHz
HSTL-I	300 MHz
HSTL-II	300 MHz
SSTL2-I	300 MHz
SSTL2-II	300 MHz
SSTL3-I	300 MHz
SSTL3-II	300 MHz
GTL+ 3.3 V	300 MHz
GTL+ 2.5 V	300 MHz
GTL 3.3 V	300 MHz
GTL 2.5 V	300 MHz
LVDS	350 MHz
LVPECL	300 MHz

Table 2-71 • Maximum I/O Frequency for Single-Ended and Differential I/Os for Advanced I/Os (maximum drive strength and high slew selected)

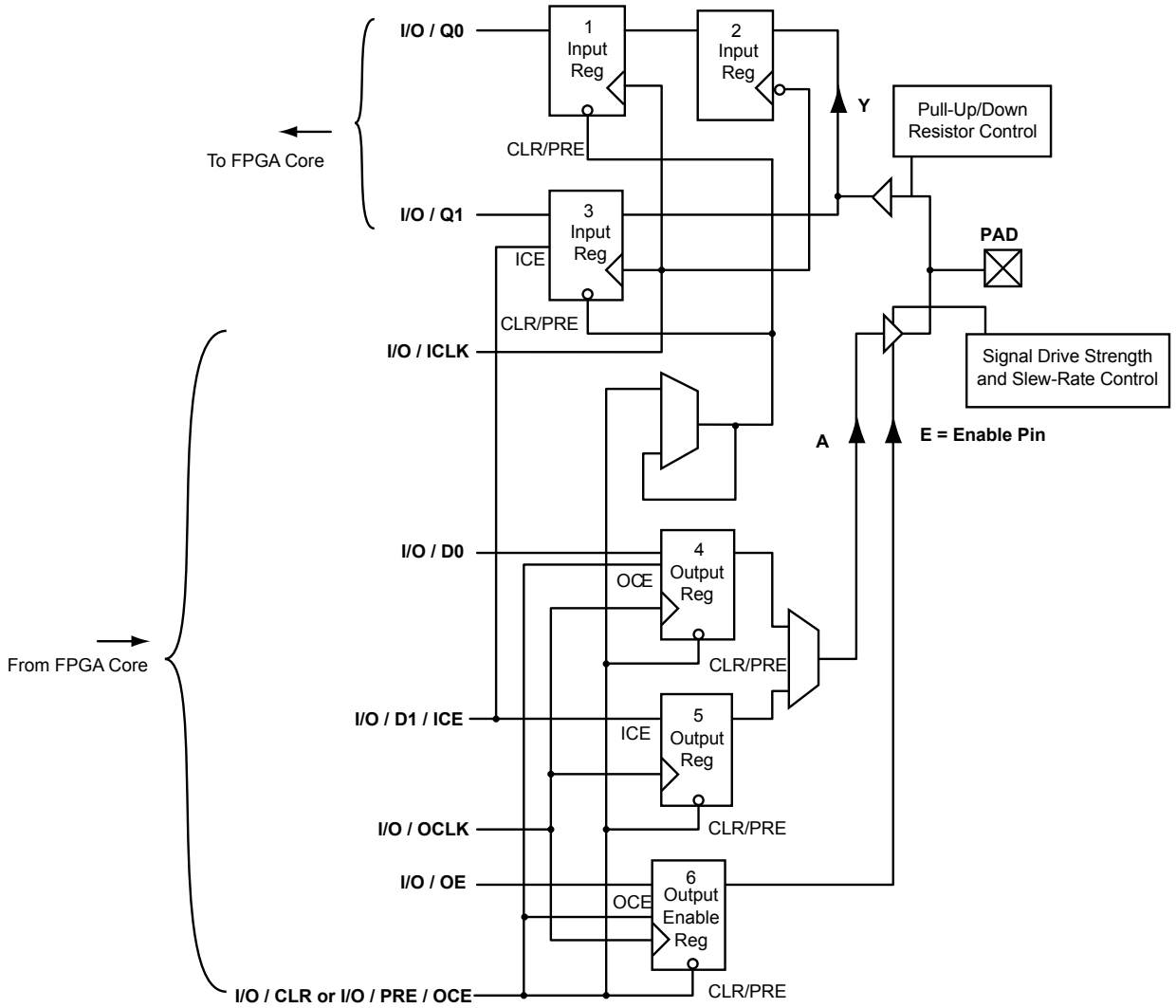
Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	250 MHz
LVCMOS 2.5 V	300 MHz
LVCMOS 1.8 V	250 MHz
LVCMOS 1.5 V	180 MHz
PCI	300 MHz
PCI-X	300 MHz
LVDS	350 MHz
LVPECL	300 MHz

I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 2-95 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 2-95) between registers to implement single or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user.

A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation. The I/O register combining must satisfy some rules.



Note: Fusion I/Os have registers to support DDR functionality (see the "Double Data Rate (DDR) Support" section on page 2-137 for more information).

Figure 2-95 • **I/O Block Logical Representation**

Double Data Rate (DDR) Support

Fusion Pro I/Os support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making it very efficient for implementing very high-speed systems.

DDR interfaces can be implemented using HSTL, SSTL, LVDS, and LVPECL I/O standards. In addition, high-speed DDR interfaces can be implemented using LVDS I/O.

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 2-96. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on Fusion devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in Figure 2-97 on page 2-138. New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Refer to the Actel application note *Using DDR for Fusion Devices* for more information.

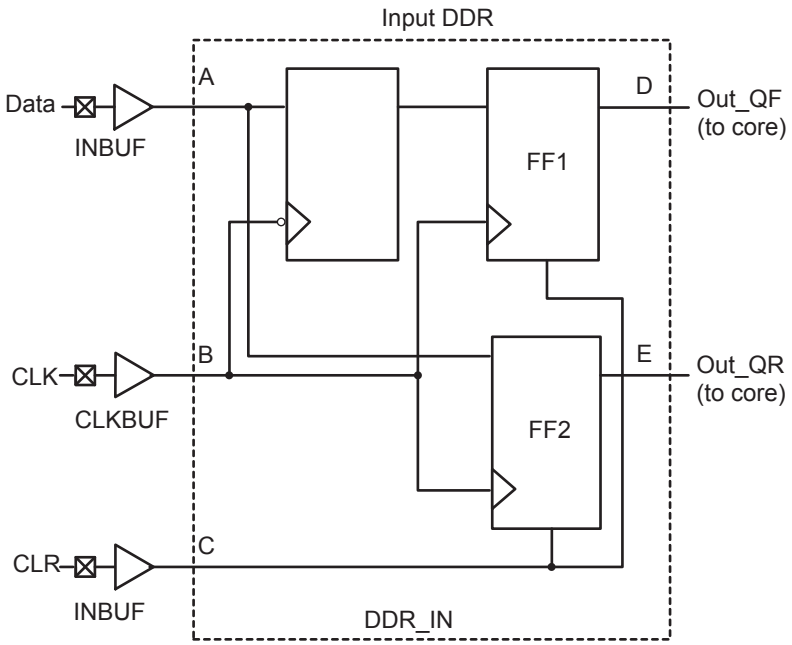


Figure 2-96 • **DDR Input Register Support in Fusion Devices**

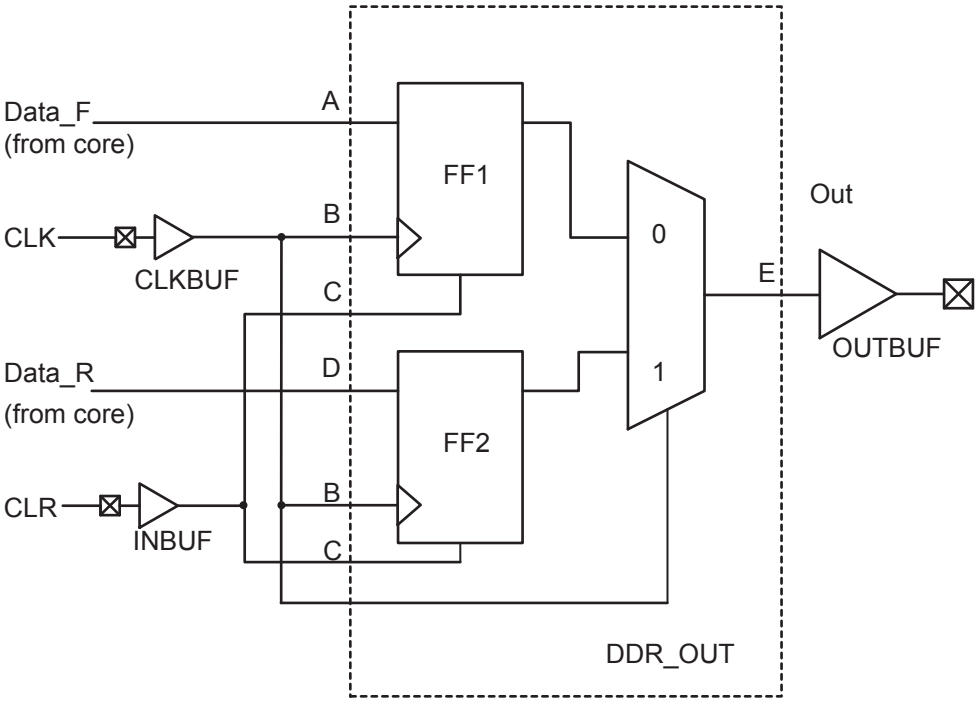


Figure 2-97 • **DDR Output Support in Fusion Devices**

Hot-Swap Support

Hot-swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in (or from) a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 2-72. The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required.

Table 2-72 • **Levels of Hot-Swap Support**

Hot Swapping Level	Description	Power Applied to Device	Bus State	Card Ground Connection	Device Circuitry Connected to Bus Pins	Example of Application with Cards that Contain Fusion Devices	Compliance of Fusion Devices
1	Cold-swap	No	–	–	–	System and card with Actel FPGA chip are powered down, then card gets plugged into system, then power supplies are turned on for system but not for FPGA on card.	Compliant I/Os can but do not have to be set to hot insertion mode.
2	Hot-swap while reset	Yes	Held in reset state	Must be made and maintained for 1 ms before, during, and after insertion/ removal	–	In PCI hot plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable.	Compliant I/Os can but do not have to be set to hot insertion mode.
3	Hot-swap while bus idle	Yes	Held idle (no ongoing I/O processes during insertion/removal)	Same as Level 2	Must remain glitch-free during power-up or power-down	Board bus shared with card bus is "frozen," and there is no toggling activity on bus. It is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode.
4	Hot-swap on an active bus	Yes	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle.	Same as Level 2	Same as Level 3	There is activity on the system bus, and it is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode.

For Fusion devices requiring Level 3 and/or Level 4 compliance, the board drivers connected to Fusion I/Os need to have 10 kΩ (or lower) output drive resistance at hot insertion, and 1 kΩ (or lower) output drive resistance at hot removal. This is the resistance of the transmitter sending a signal to the Fusion I/O, and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to meet Level 3 and/or Level 4 compliance. Cards with two levels of staging should have the following sequence:

1. Grounds
2. Powers, I/Os, other pins

Cold-Sparing Support

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

Pro I/O banks fully support cold-sparing.

For Pro I/O banks, standards such as PCI that require I/O clamp diodes, can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

For Advanced I/O banks, since the I/O clamp diode is always active, cold-sparing can be accomplished either by employing a bus switch to isolate the device I/Os from the rest of the system or by driving each advanced I/O pin to 0 V.

If a resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitor is in parallel with the resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

I/O cold-sparing may add additional current if the pin is configured with either a pull-up or pull-down resistor and driven in the opposite direction. A small static current is induced on each I/O pin when the pin is driven to a voltage opposite to the weak pull resistor. The current is equal to the voltage drop across the input pin divided by the pull resistor. Refer to Table 2-90 on page 2-166, Table 2-91 on page 2-166, and Table 2-92 on page 2-168 for the specific pull resistor value for the corresponding I/O standard.

For example, assuming an LVTTL 3.3 V input pin is configured with a weak Pull-up resistor, a current will flow through the pull-up resistor if the input pin is driven low. For an LVTTL 3.3 V, pull-up resistor is ~45 kΩ and the resulting current is equal to 3.3 V / 45 kΩ = 73 µA for the I/O pin. This is true also when a weak pull-down is chosen and the input pin is driven high. Avoiding this current can be done by driving the input low when a weak pull-down resistor is used, and driving it high when a weak pull-up resistor is used.

In Active and Static modes, this current draw can occur in the following cases:

- Input buffers with pull-up, driven Low
- Input buffers with pull-down, driven High
- Bidirectional buffers with pull-up, driven Low
- Bidirectional buffers with pull-down, driven High
- Output buffers with pull-up, driven Low
- Output buffers with pull-down, driven High
- Tristate buffers with pull-up, driven Low
- Tristate buffers with pull-down, driven High

Electrostatic Discharge (ESD) Protection

Fusion devices are tested per JEDEC Standard JESD22-A114-B.

Fusion devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to VCCI. The second diode has its P side connected to GND and its N side connected to the pad. During operation, these diodes are normally biased in the Off state, except when transient voltage is significantly above VCCI or below GND levels.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to Table 2-73 and Table 2-74 for more information about I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

Table 2-73 • **Fusion Advanced I/Os – Hot-Swap and 5 V Input Tolerance Capabilities**

I/O Assignment	Clamp Diode	Hot Insertion	5 V Input Tolerance [1]	Input Buffer	Output Buffer
3.3 V LVTTL/LVCMOS	Yes	No	Yes[1]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes[1]	Enabled/Disabled	
LVCMOS 2.5 V	Yes	No	No	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V	Yes	No	Yes[2]	Enabled/Disabled	
LVCMOS 1.8 V	Yes	No	No	Enabled/Disabled	
LVCMOS 1.5 V	Yes	No	No	Enabled/Disabled	
Differential, LVDS/B-LVDS/M-LVDS/ LVPECL [3]	Yes	No	No	Enabled/Disabled	

Notes:

1. *Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.*
2. *Can be implemented with an external resistor and an internal clamp diode.*
3. *Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.*

Table 2-74 • **Fusion Pro I/Os – Hot-Swap and 5 V Input Tolerance Capabilities**

I/O Assignment	Clamp Diode	Hot Insertion	5 V Input Tolerance	Input Buffer	Output Buffer
3.3 V LVTTL/LVCMOS	No	Yes	Yes[1]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes[1]	Enabled/Disabled	
LVCMOS 2.5 V [3]	No	Yes	No	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V [3]	Yes	No	Yes[2]	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.5 V	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/B-LVDS/M-LVDS/LVPECL[4]	No	Yes	No	Enabled/Disabled	

Notes:

1. *Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.*
2. *Can be implemented with an external resistor and an internal clamp diode.*
3. *In the SmartGen, FlashROM, Flash Memory System Builder, and Analog System Builder User's Guide, select the LVCMOS5 macro for the LVCMOS 2.5 V / 5.0 V I/O standard or the LVCMOS25 macro for the LVCMOS 2.5 V I/O standard.*
4. *Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.*

5 V Input Tolerance

I/Os can support 5 V input tolerance when LVTTL 3.3 V, LVCMOS 3.3 V, LVCMOS 2.5 V / 5 V, and LVCMOS 2.5 V configurations are used (see Table 2-75 on page 2-145 for more details). There are four recommended solutions (see Figure 2-98 to Figure 2-101 on page 2-144 for details of board and macro setups) to achieve 5 V receiver tolerance. All the solutions meet a common requirement of limiting the voltage at the input to 3.6 V or less. In fact, the I/O absolute maximum voltage rating is 3.6 V, and any voltage above 3.6 V may cause long-term gate oxide failures.

Solution 1

The board-level design needs to ensure that the reflected waveform at the pad does not exceed the limits provided in Table 3-4 on page 3-5. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI / PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the two external resistors, as explained below. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

The following are some examples of possible resistor values (based on a simplified simulation model with no line effects and 10 Ω transmitter output resistance, where Rtx_out_high = (VCCI – VOH) / I_{OH}, Rtx_out_low = VOL / I_{OL}).

Example 1 (high speed, high current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 36 Ω (±5%), P(r1)min = 0.069 Ω

R2 = 82 Ω (±5%), P(r2)min = 0.158 Ω

Imax_tx = 5.5 V / (82 * 0.95 + 36 * 0.95 + 10) = 45.04 mA

t_{RISE} = t_{FALL} = 0.85 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Example 2 (low–medium speed, medium current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 220 Ω (±5%), P(r1)min = 0.018 Ω

R2 = 390 Ω (±5%), P(r2)min = 0.032 Ω

Imax_tx = 5.5 V / (220 * 0.95 + 390 * 0.95 + 10) = 9.17 mA

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 20 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Other values of resistors are also allowed as long as the resistors are sized appropriately to limit the voltage at the receiving end to 2.5 V < Vin(rx) < 3.6 V when the transmitter sends a logic 1. This range of Vin_dc(rx) must be assured for any combination of transmitter supply (5 V ± 0.5 V), transmitter output resistance, and board resistor tolerances.

Temporary overshoots are allowed according to Table 3-4 on page 3-5.

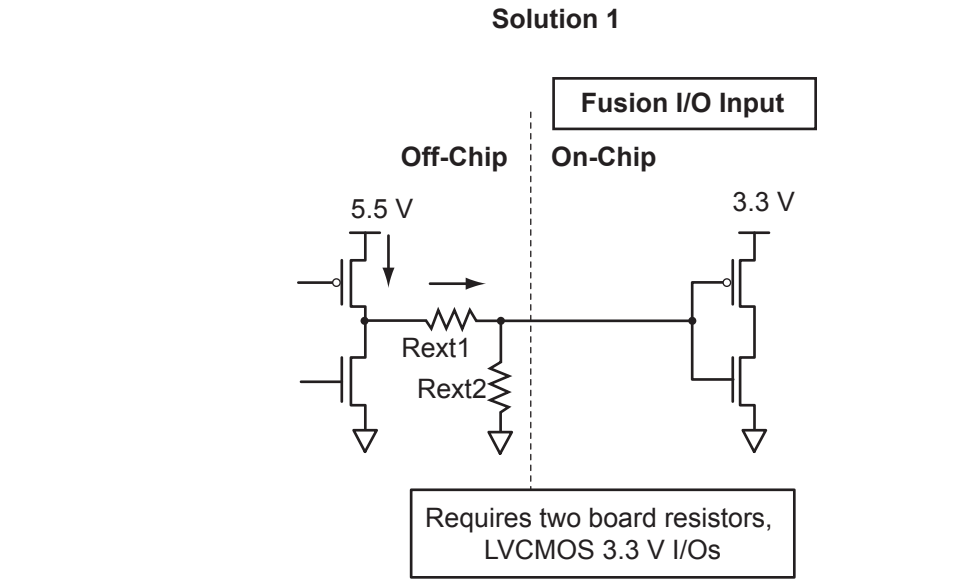


Figure 2-98 • **Solution 1**

Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-5. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in Figure 2-99. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

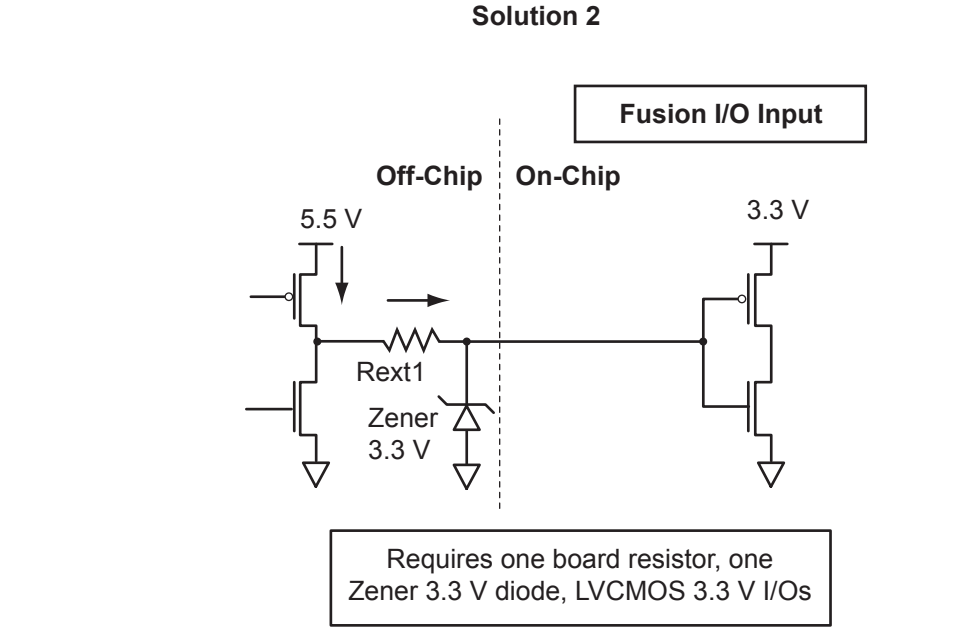


Figure 2-99 • **Solution 2**

Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-5. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 2-100. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

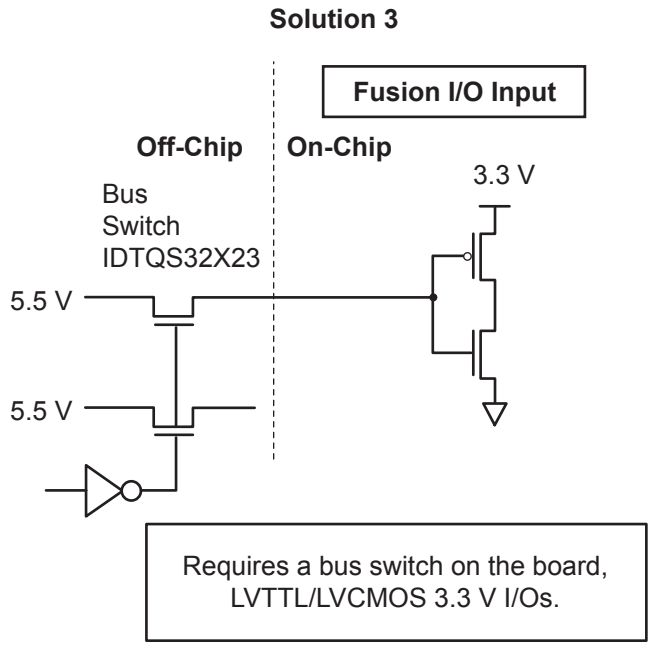


***Figure 2-100* • Solution 3**

Solution 4

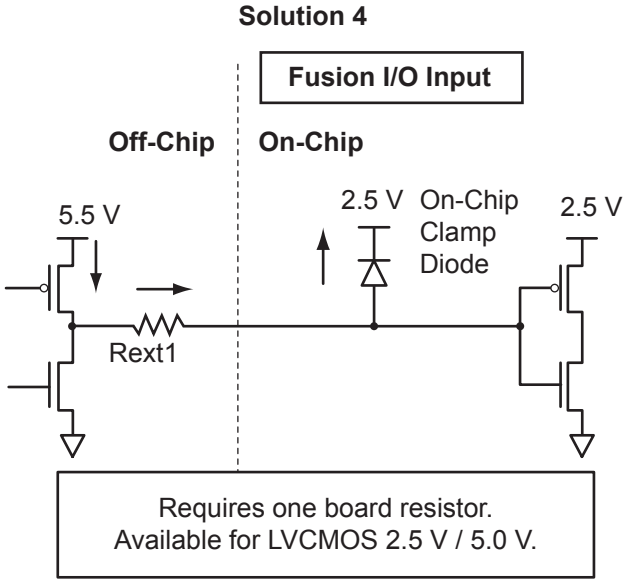


***Figure 2-101* • Solution 4**

Table 2-75 • **Comparison Table for 5 V–Compliant Receiver Scheme**

Scheme	Board Components	Speed	Current Limitations
1	Two resistors	Low to high[1]	Limited by transmitter's drive strength
2	Resistor and Zener 3.3 V	Medium	Limited by transmitter's drive strength
3	Bus switch	High	N/A
4	Minimum resistor value[2] R = 47 Ω at T_J = 70°C R = 150 Ω at T_J = 85°C R = 420 Ω at T_J = 100°C	Medium	Maximum diode current at 100% duty cycle, signal constantly at '1' 52.7 mA at T_J =70°C / 10-year lifetime 16.5 mA at T_J = 85°C / 10-year lifetime 5.9 mA at T_J = 100°C / 10-year lifetime For duty cycles other than 100%, the currents can be increased by a factor = 1 / (duty cycle). Example: 20% duty cycle at 70°C Maximum current = (1 / 0.2) * 52.7 mA = 5 * 52.7 mA = 263.5 mA

Notes:

1. *Speed and current consumption increase as the board resistance values decrease.*
2. *Resistor values ensure I/O diode long-term reliability.*

5 V Output Tolerance

Fusion I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, Fusion I/Os can directly drive signals into 5 V TTL receivers. In fact, VOL = 0.4 V and VOH = 2.4 V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceed the VIL = 0.8 V and VIH = 2 V level requirements of 5 V TTL receivers. Therefore, level '1' and level '0' will be recognized correctly by 5 V TTL receivers.

Simultaneously Switching Outputs and PCB Layout

Simultaneously switching outputs (SSOs) can produce signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and VCCI dip noise. These two noise types are caused by rapidly changing currents through GND and VCCI package pin inductances during switching activities:

- Ground bounce noise voltage = L(GND) * di/dt
- VCCI dip noise voltage = L(VCCI) * di/dt

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

Selectable Skew between Output Buffer Enable/Disable Time

The configurable skew block is used to delay the output buffer assertion (enable) without affecting deassertion (disable) time.

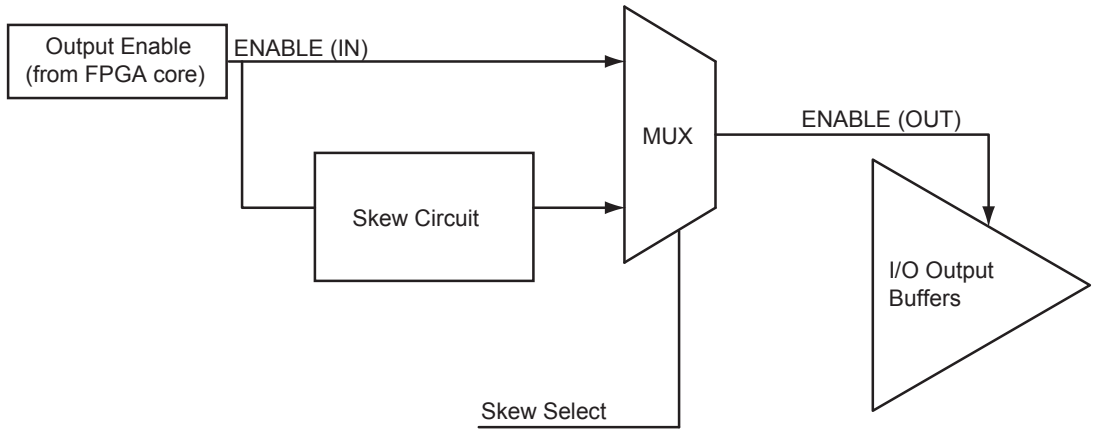


***Figure 2-102* • Block Diagram of Output Enable Path**

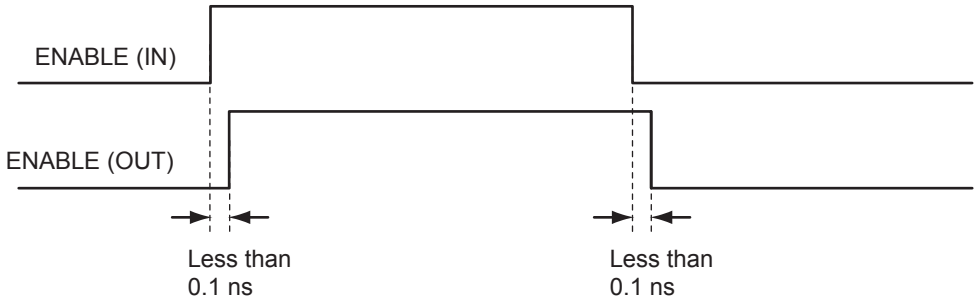


***Figure 2-103* • Timing Diagram (option1: bypasses skew circuit)**

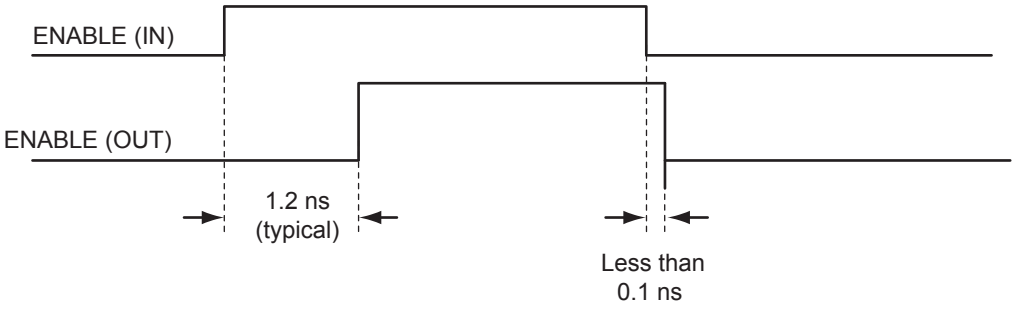


***Figure 2-104* • Timing Diagram (option 2: enables skew circuit)**

At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss or transmitter overstress due to transmitter-to-transmitter current shorts. Figure 2-105 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-106 shows how bus contention is created, and Figure 2-107 on page 2-149 shows how it can be avoided with the skew circuit.

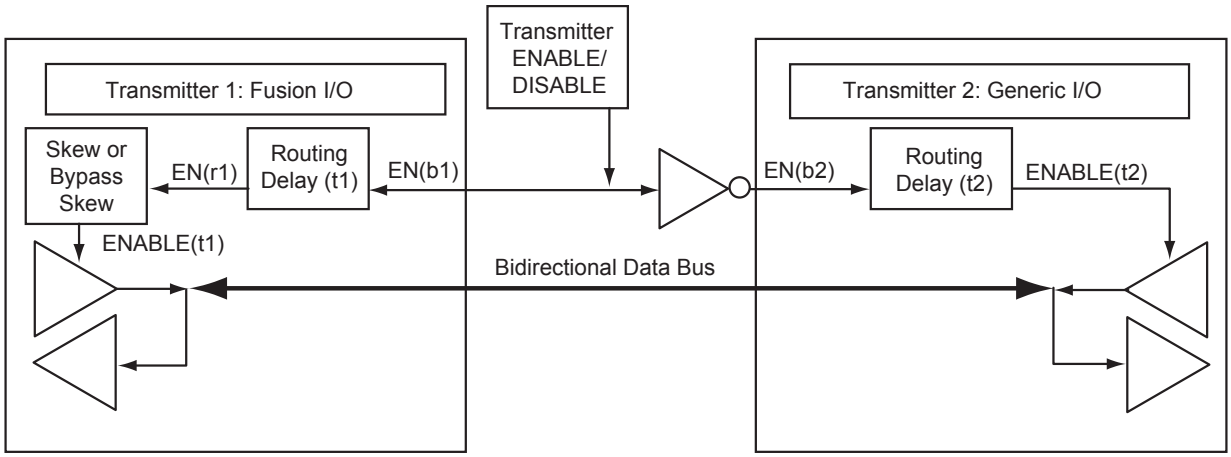


***Figure 2-105* • Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using Fusion Devices**

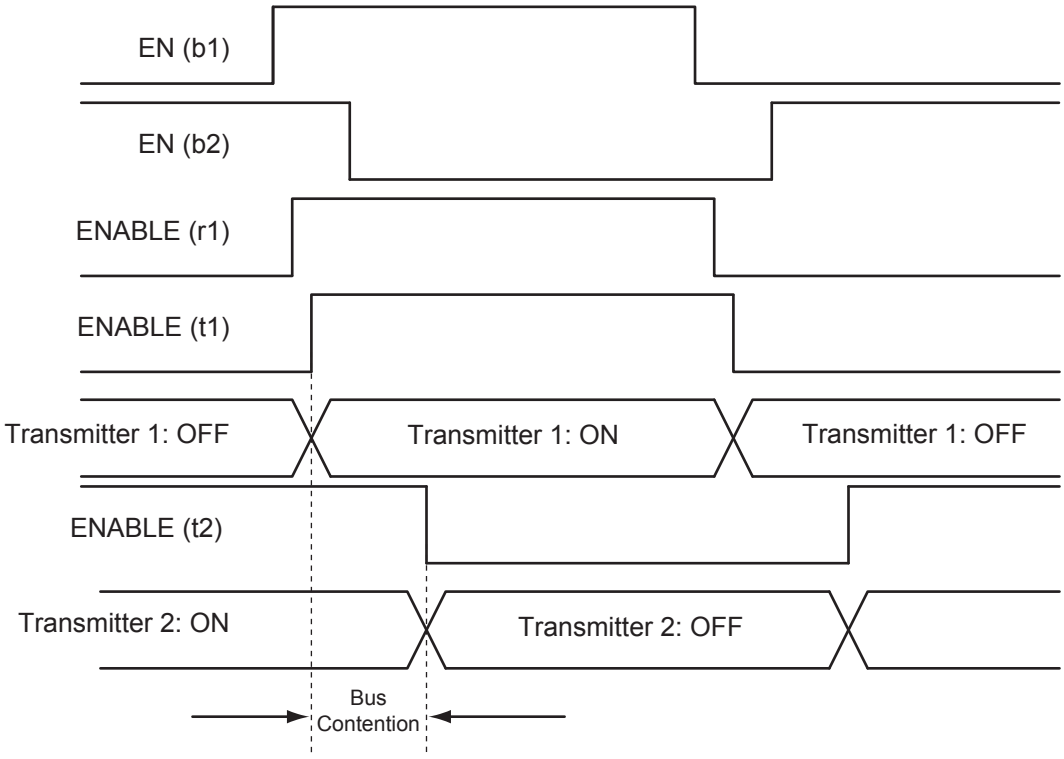


***Figure 2-106* • Timing Diagram (bypasses skew circuit)**

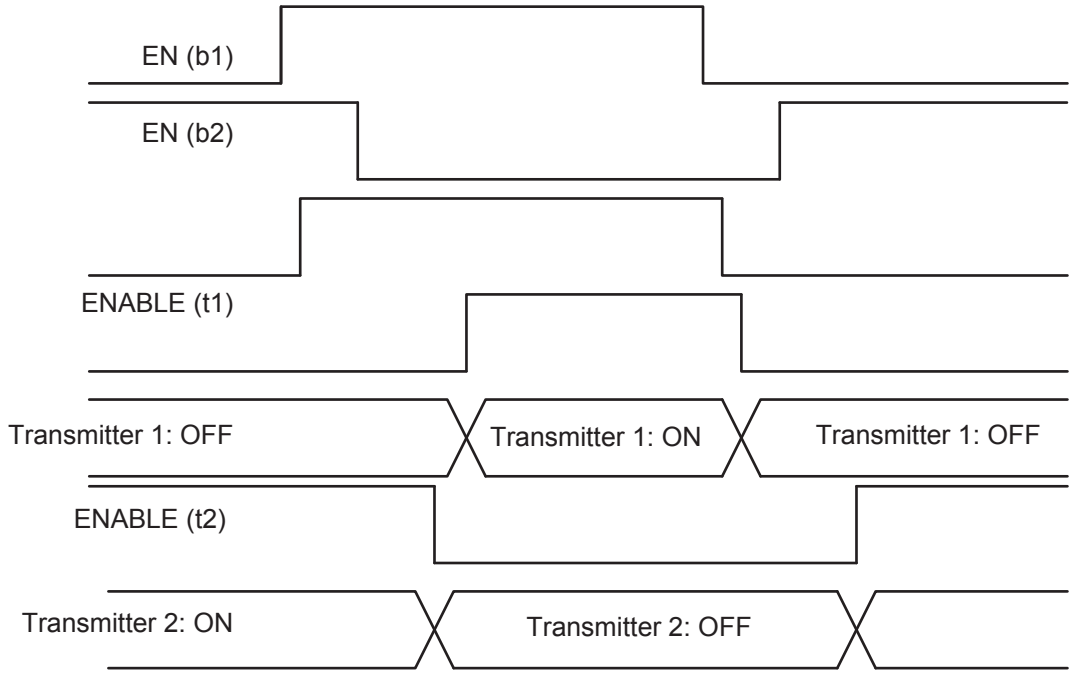


***Figure 2-107* • Timing Diagram (with skew circuit selected)**

Weak Pull-Up and Weak Pull-Down Resistors

Fusion devices support optional weak pull-up and pull-down resistors for each I/O pin. When the I/O is pulled up, it is connected to the VCCI of its corresponding I/O bank. When it is pulled down, it is connected to GND. Refer to Table 2-92 on page 2-168 for more information.

Slew Rate Control and Drive Strength

Fusion devices support output slew rate control: high and low. The high slew rate option is recommended to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. Low slew rate is recommended when bus transients are expected. Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 2.5 V / 5.0 V input, LVCMOS 1.8 V, and LVCMOS 1.5 V. All other I/O standards have a high output slew rate by default.

For Fusion slew rate and drive strength specifications, refer to the appropriate I/O bank table:

- Fusion Advanced I/O (Table 2-76 on page 2-150)
- Fusion Pro I/O (Table 2-77 on page 2-150)

Table 2-80 on page 2-153 lists the default values for the above selectable I/O attributes as well as those that are preset for each I/O standard.

Refer to Table 2-76 and Table 2-77 for SLEW and OUT_DRIVE settings. Table 2-78 on page 2-151 and Table 2-79 on page 2-152 list the I/O default attributes. Table 2-80 on page 2-153 lists the voltages for the supported I/O standards.

Table 2-76 • **Fusion Advanced I/O Standards—SLEW and OUT_DRIVE Settings**

	OUT_DRIVE (mA)							
I/O Standards	**2**	**4**	**6**	**8**	**12**	**16**	**Slew**	
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓	✓	✓	✓	–	High	Low
LVCMOS 1.8 V	✓	✓	✓	✓	–	–	High	Low
LVCMOS 1.5 V	✓	✓	–	–	–	–	High	Low

Table 2-77 • **Fusion Pro I/O Standards—SLEW and OUT_DRIVE Settings**

	OUT_DRIVE (mA)								
I/O Standards	**2**	**4**	**6**	**8**	**12**	**16**	**24**	**Slew**	
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V/5.0 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓	–	High	Low
LVCMOS 1.5 V	✓	✓	✓	✓	✓	–	–	High	Low

Table 2-78 • **Fusion Pro I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)
LVTTL/LVCMOS 3.3 V	Refer to the following tables for more information: Table 2-76 on page 2-150 Table 2-77 on page 2-150	Refer to the following tables for more information: Table 2-76 on page 2-150 Table 2-77 on page 2-150	Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5/5.0 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.8 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.5 V			Off	None	35 pF	–	Off	0	Off
PCI (3.3 V)			Off	None	10 pF	–	Off	0	Off
PCI-X (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (2.5 V)			Off	None	10 pF	–	Off	0	Off
GTL (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL (2.5 V)			Off	None	10 pF	–	Off	0	Off
HSTL Class I			Off	None	20 pF	–	Off	0	Off
HSTL Class II			Off	None	20 pF	–	Off	0	Off
SSTL2 Class I and II			Off	None	30 pF	–	Off	0	Off
SSTL3 Class I and II			Off	None	30 pF	–	Off	0	Off
LVDS, B-LVDS, M-LVDS			Off	None	0 pF	–	Off	0	Off
LVPECL			Off	None	0 pF	–	Off	0	Off

Table 2-79 • **Advanced I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	Refer to the following tables for more information: Table 2-76 on page 2-150 Table 2-77 on page 2-150	Refer to the following tables for more information: Table 2-76 on page 2-150 Table 2-77 on page 2-150	Off	None	35 pF	–
LVCMOS 2.5 V			Off	None	35 pF	–
LVCMOS 2.5/5.0 V			Off	None	35 pF	–
LVCMOS 1.8 V			Off	None	35 pF	–
LVCMOS 1.5 V			Off	None	35 pF	–
PCI (3.3 V)			Off	None	10 pF	–
PCI-X (3.3 V)			Off	None	10 pF	–
LVDS, B-LVDS, M-LVDS			Off	None	–	–
LVPECL			Off	None	–	–

Table 2-80 • Fusion Pro I/O Supported Standards and Corresponding VREF and VTT Voltages Applicable to all I/O Bank types

I/O Standard	Input/Output Supply Voltage (VMVtyp/VCCI_TYP)	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_TYP)
LVTTL/LVCMOS 3.3 V	3.30 V	–	–
LVCMOS 2.5 V	2.50 V	–	–
LVCMOS 2.5 V / 5.0 V Input	2.50 V	–	–
LVCMOS 1.8 V	1.80 V	–	–
LVCMOS 1.5 V	1.50 V	–	–
PCI 3.3 V	3.30 V	–	–
PCI-X 3.3 V	3.30 V	–	–
GTL+ 3.3 V	3.30 V	1.00 V	1.50 V
GTL+ 2.5 V	2.50 V	1.00 V	1.50 V
GTL 3.3 V	3.30 V	0.80 V	1.20 V
GTL 2.5 V	2.50 V	0.80 V	1.20 V
HSTL Class I	1.50 V	0.75 V	0.75 V
HSTL Class II	1.50 V	0.75 V	0.75 V
SSTL3 Class I	3.30 V	1.50 V	1.50 V
SSTL3 Class II	3.30 V	1.50 V	1.50 V
SSTL2 Class I	2.50 V	1.25 V	1.25 V
SSTL2 Class II	2.50 V	1.25 V	1.25 V
LVDS	2.50 V	–	–
LVPECL	3.30 V	–	–

I/O Software Support

In the Fusion development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-81 and Table 2-82 on page 2-155 list the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in Fusion support up to five different drive strengths.

Table 2-81 • **Fusion Advanced I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓
LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓
LVCMOS 1.5 V	✓	✓	✓	✓	✓	✓
PCI (3.3 V)			✓		✓	✓
PCI-X (3.3 V)	✓		✓		✓	✓
LVDS, B-LVDS, M-LVDS			✓			✓
LVPECL						✓

Table 2-82 • **Fusion Pro I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)	HOT_SWAPPABLE
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 1.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI (3.3 V)			✓		✓	✓	✓	✓		
PCI-X (3.3 V)	✓		✓		✓	✓	✓	✓		
GTL+ (3.3 V)			✓		✓	✓	✓	✓		✓
GTL+ (2.5 V)			✓		✓	✓	✓	✓		✓
GTL (3.3 V)			✓		✓	✓	✓	✓		✓
GTL (2.5 V)			✓		✓	✓	✓	✓		✓
HSTL Class I			✓		✓	✓	✓	✓		✓
HSTL Class II			✓		✓	✓	✓	✓		✓
SSTL2 Class I and II			✓		✓	✓	✓	✓		✓
SSTL3 Class I and II			✓		✓	✓	✓	✓		✓
LVDS, B-LVDS, M-LVDS			✓			✓	✓	✓		✓
LVPECL						✓	✓	✓		✓

User I/O Naming Convention

Due to the comprehensive and flexible nature of Fusion device user I/Os, a naming scheme is used to show the details of the I/O (Figure 2-108). The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwByVz

Gmn is only used for I/Os that also have CCC access—i.e., global pins.

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle).

n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2. Figure 2-22 on page 2-25 shows the three input pins per clock source MUX at CCC location m.

u = I/O pair number in the bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.

x = P (Positive) or N (Negative) for differential pairs, or R (Regular – single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only. U (Positive-LVDS only) or V (Negative-LVDS only) restrict the I/O differential pair from being selected as an LVPECL pair.

w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number (0–3). The Bank number starts at 0 from the northwest I/O bank and proceeds in a clockwise direction.

V = Reference voltage

z = Minibank number

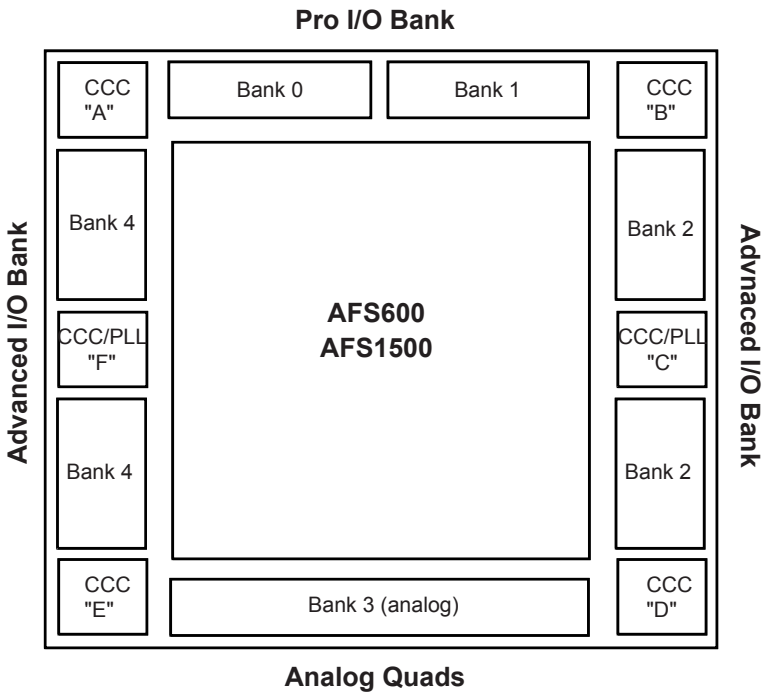


***Figure 2-108* • Naming Conventions of Fusion Devices with Four I/O Banks**

User I/O Characteristics

Timing Model

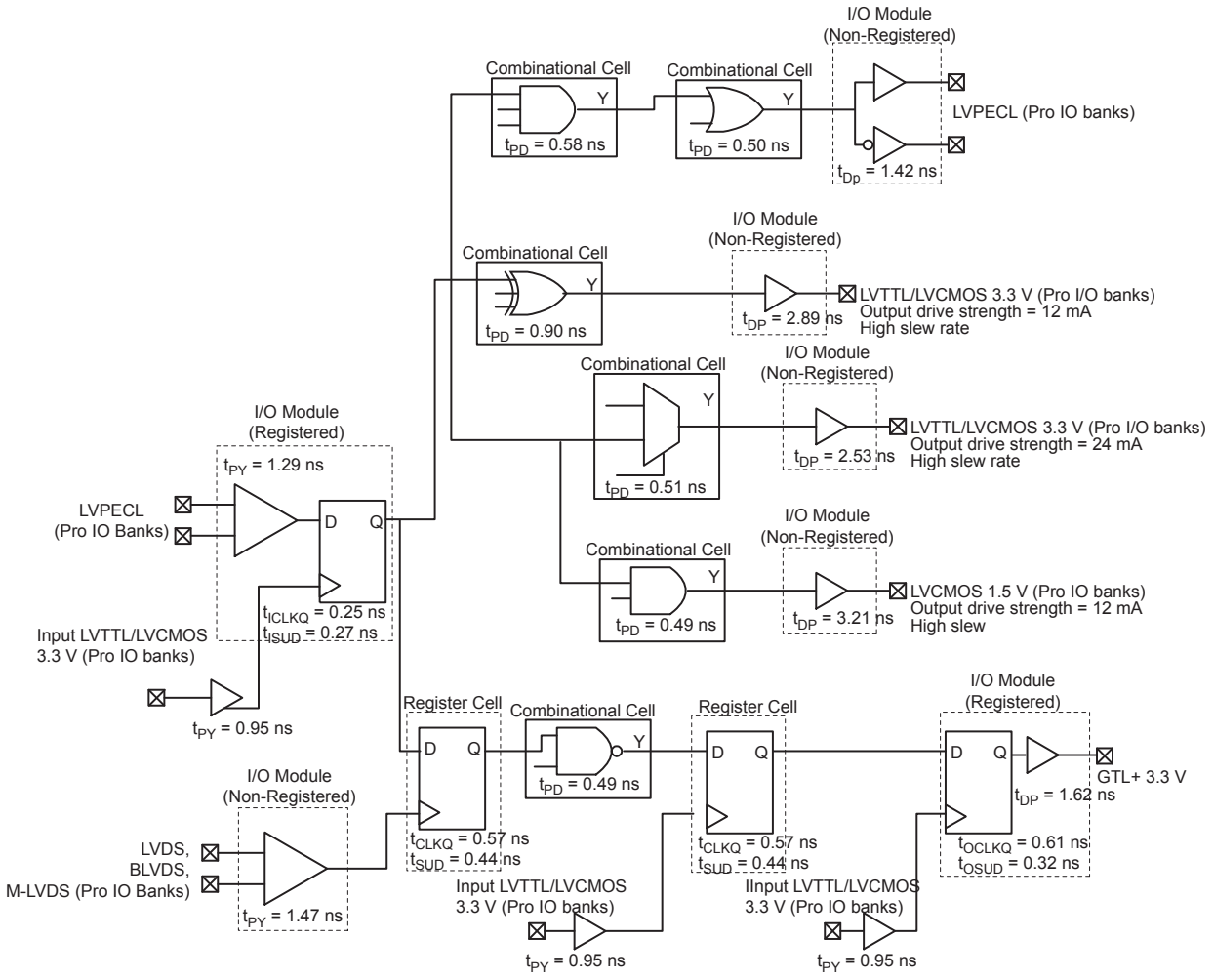


***Figure 2-109* • Timing Model**
Operating Conditions: –2 Speed, Extended Temperature Range (T_J = 100°C), Worst-Case VCC = 1.425 V

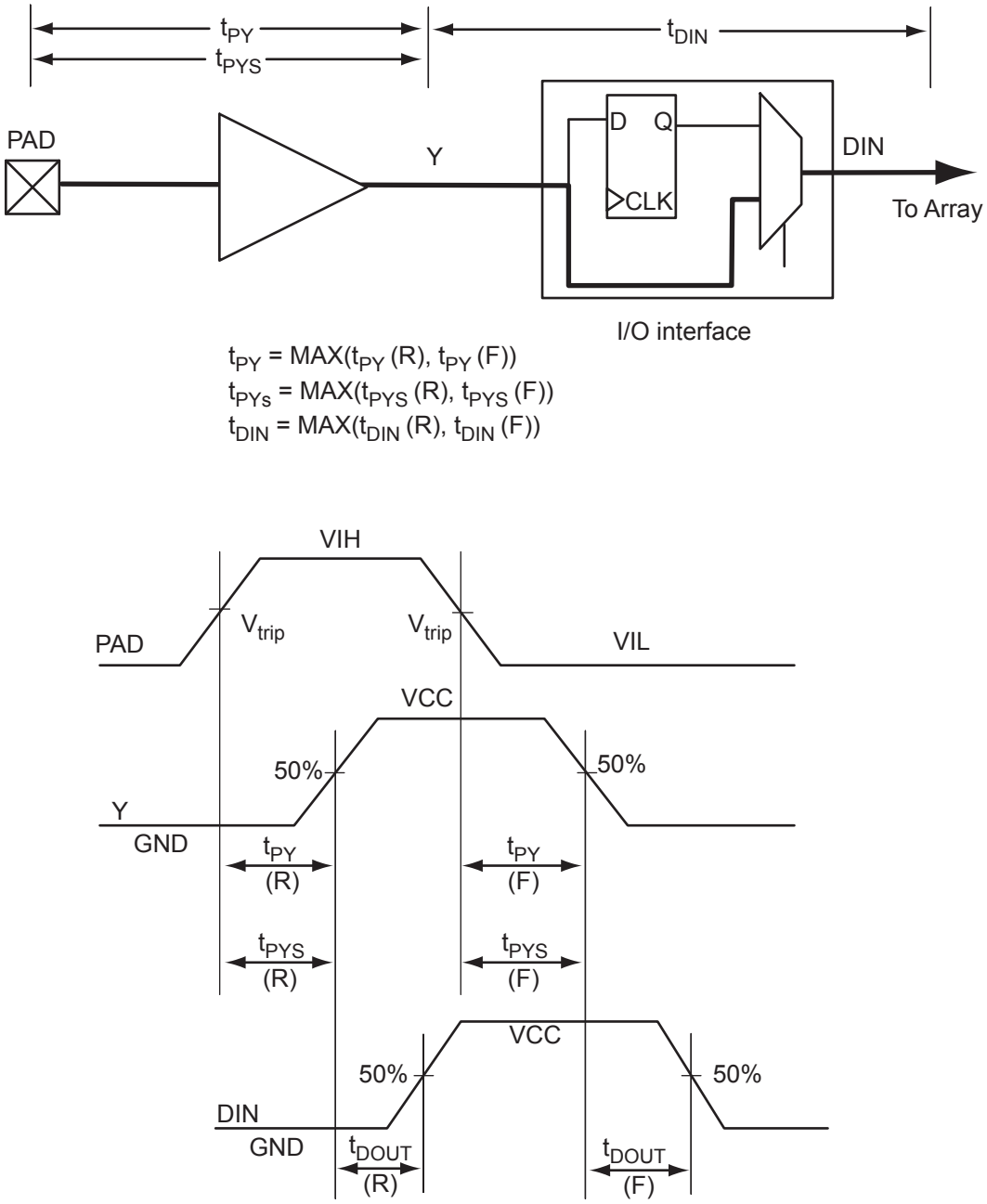


***Figure 2-110* • Input Buffer Timing Model and Delays (example)**

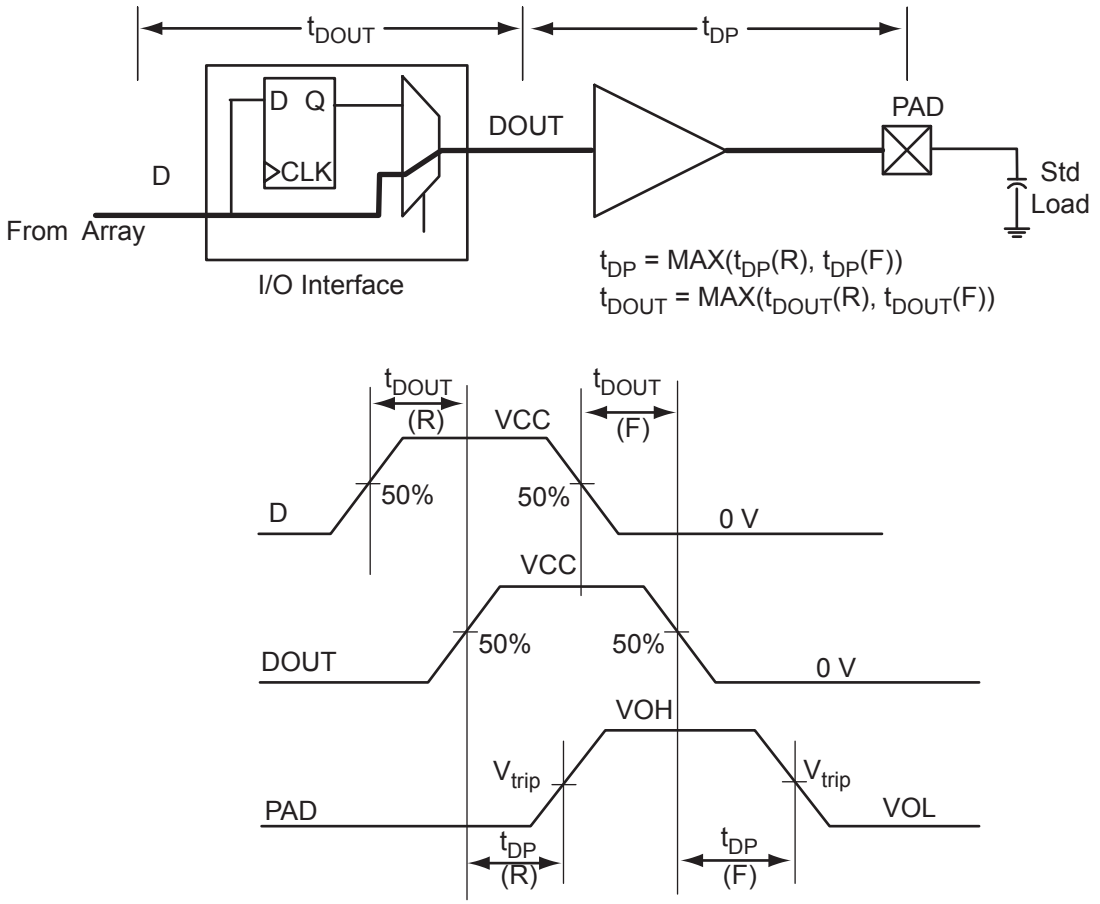


***Figure 2-111* • Output Buffer Model and Delays (example)**

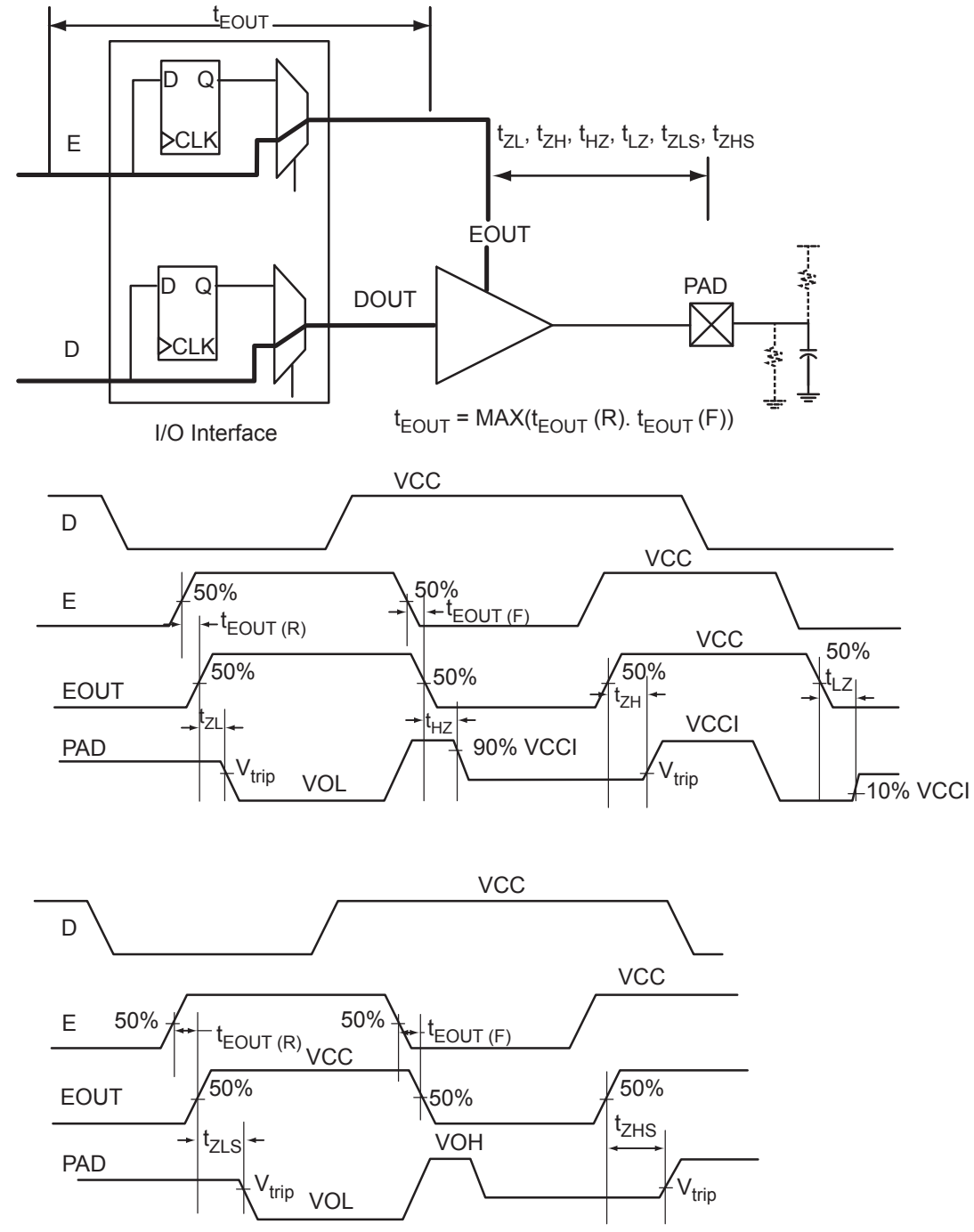


***Figure 2-112* • Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Extended Temperature Conditions Applicable to Pro I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	25 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	25	25
2.5 V GTL	25 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	25	25
3.3 V GTL+	35 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA[2]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *Currents are measured at 100°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*
3. *Output slew rate can be extracted by the IBIS models.*

Table 2-84 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Extended Temperature Conditions Applicable to Advanced I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 100°C junction temperature.

Table 2-85 • Summary of Maximum and Minimum DC Input Levels Applicable to Extended Temperature Conditions in all I/O Bank Types

	Extended Temperature (K)[1]	
	I_{IL}[2]	I_{IL}[3]
DC I/O Standards	**µA**	**µA**
3.3 V LVTTL / 3.3 V LVCMOS	15	15
2.5 V LVCMOS	15	15
1.8 V LVCMOS	15	15
1.5 V LVCMOS	15	15
3.3 V PCI	15	15
3.3 V PCI-X	15	15
3.3 V GTL	15	15
2.5 V GTL	15	15
3.3 V GTL+	15	15
2.5 V GTL+	15	15
HSTL (I)	15	15
HSTL (II)	15	15
SSTL2 (I)	15	15
SSTL2 (II)	15	15
SSTL3 (I)	15	15
SSTL3 (II)	15	15

Notes:

1. *Extended Temperature range (–55°C < T_J < 100°C)*
2. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-86 • Summary of AC Measuring Points Applicable to All I/O Bank Types

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 2-87 • I/O AC Parameter Definitions

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Table 2-88 • Summary of I/O Timing Characteristics – Software Default Settings, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI as Per Configuration Applicable to Pro I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTL/ 3.3 V LVCMOS	12 mA	High	35	–	0.51	2.89	0.03	0.95	1.23	0.33	2.94	2.26	2.58	2.85	4.70	4.02	ns
2.5 V LVCMOS	12 mA	High	35	–	0.51	2.95	0.03	1.19	1.31	0.33	3.00	2.75	2.65	2.75	4.76	4.51	ns
1.8 V LVCMOS	12 mA	High	35	–	0.51	2.99	0.03	1.14	1.50	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns
1.5 V LVCMOS	12 mA	High	35	–	0.51	3.21	0.03	1.13	1.69	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns
3.3 V PCI	Per PCI spec	High	10	25 [2]	0.51	2.21	0.03	0.83	1.32	0.33	2.25	1.57	2.58	2.85	4.01	3.33	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 [2]	0.51	2.21	0.03	0.81	1.24	0.33	2.25	1.57	2.58	2.85	4.01	3.33	ns
3.3 V GTL	25 mA	High	10	25	0.51	1.63	0.03	2.31	–	0.33	1.60	1.63			3.36	3.40	ns
2.5 V GTL	25 mA	High	10	25	0.51	1.68	0.03	1.93	–	0.33	1.70	1.68			3.46	3.44	ns
3.3 V GTL+	35 mA	High	10	25	0.51	1.62	0.03	1.25	–	0.33	1.65	1.62			3.41	3.38	ns
2.5 V GTL+	33mA	High	10	25	0.51	1.74	0.03	1.19	–	0.33	1.77	1.65			3.53	3.41	ns
HSTL (I)	8 mA	High	20	50	0.51	2.50	0.03	1.67	–	0.33	2.55	2.48			4.31	4.24	ns
HSTL (II)	15 mA	High	20	25	0.51	2.38	0.03	1.67	–	0.33	2.43	2.14			4.19	3.90	ns
SSTL2 (I)	17 mA	High	30	50	0.51	1.68	0.03	1.05	–	0.33	1.71	1.45			3.47	3.22	ns
SSTL2 (II)	21 mA	High	30	25	0.51	1.71	0.03	1.05	–	0.33	1.74	1.39			3.50	3.15	ns
SSTL3 (I)	16 mA	High	30	50	0.51	1.82	0.03	0.99	–	0.33	1.85	1.45			3.61	3.21	ns
SSTL3 (II)	24 mA	High	30	25	0.51	1.63	0.03	0.99	–	0.33	1.66	1.32			3.42	3.08	ns
LVDS	24 mA	High	–	–	0.51	1.48	0.03	1.47	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.51	1.42	0.03	1.29	–	–	–	–	–	–	–	–	ns

Notes:

1. *For the derating values at specific junction temperature and voltage-supply levels, refer to Table 3-7 on page 3-10.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-96 on page 2-137 for connectivity. This resistor is not required during normal operation.*

Table 2-89 • Summary of I/O Timing Characteristics – Software Default Settings, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI as Per Configuration Applicable to Advanced I/O banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{HZLS}	t_{HZHS}	Units
3.3 V LVTTL/ 3.3 V LVCMOS	12 mA	High	35	–	0.51	2.78	0.03	0.95	0.33	2.83	2.22	2.53	2.82	4.59	3.99	ns
2.5 V LVCMOS	12 mA	High	35	–	0.51	2.80	0.03	1.03	0.33	2.86	2.70	2.60	2.71	4.62	4.46	ns
1.8 V LVCMOS	12 mA	High	35	–	0.51	2.99	0.03	1.14	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns
1.5 V LVCMOS	12 mA	High	35	–	0.51	3.48	0.03	1.45	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns
3.3 V PCI	Per PCI spec	High	10	25 [2]	0.51	2.11	0.03	0.68	0.33	2.15	1.54	2.53	2.82	3.91	3.30	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 [2]	0.51	2.11	0.03	0.66	0.33	2.15	1.54	2.53	2.82	3.91	3.30	ns
LVDS	24 mA	High	–	–	0.51	1.48	0.03	1.31	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.51	1.42	0.00	0.00	–	–	–	–	–	–	–	ns

1. *For specific junction temperature and voltage-supply levels, refer to Table 3-7 on page 3-10 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-117 on page 2-192 for connectivity. This resistor is not required during normal operation.*

Detailed I/O DC Characteristics

Table 2-90 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
CIN	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
CINCLK	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-91 • I/O Output Buffer Maximum Resistances [1]

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (ohms) [2]	$R_{PULL\text{-}UP}$ (ohms) [3]
Applicable to Pro I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	25 mA	11	–
2.5 V GTL	25 mA	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website: www.actel.com/techdocs/models/ibis.html.*
2. *R(PULL-DOWN-MAX) = VOLspec / IOLspec*
3. *R(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec*

Table 2-91 • **I/O Output Buffer Maximum Resistances [1] (continued)**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (ohms) [2]	$R_{PULL\text{-}UP}$ (ohms) [3]
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	17 mA	27	31
SSTL2 (II)	21 mA	13	15
SSTL3 (I)	16 mA	44	69
SSTL3 (II)	24 mA	18	32
Applicable to Advanced I/O Banks			
Standard	**Drive Strength**	**RPULL-DOWN (Ω)[2]**	**RPULL-UP (Ω)[3]**
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website: www.actel.com/techdocs/models/ibis.html.*
2. *R(PULL-DOWN-MAX) = VOLspec / IOLspec*
3. *R(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec*

Table 2-91 • I/O Output Buffer Maximum Resistances [1] (continued)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (ohms) [2]	$R_{PULL\text{-}UP}$ (ohms) [3]
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website: www.actel.com/techdocs/models/ibis.html.*
2. *R(PULL-DOWN-MAX) = VOLspec / IOLspec*
3. *R(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec*

Table 2-92 • I/O Weak Pull-Up/Pull-Down Resistances, Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	R(WEAK PULL-UP) [1] (ohms)		R(WEAK PULL-DOWN) [2] (ohms)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. *R(WEAK PULL-DOWN-MAX) = VOLspec / IWEAK PULL-DOWN-MIN*
2. *R(WEAK PULL-UP-MAX) = (VCCImax – VOHspec) / IWEAK PULL-UP-MIN*

Table 2-93 • **I/O Short Currents IOSH/IOSL**

	Drive Strength	IOSH (mA)*	IOSL (mA)*
Applicable to Pro I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
Applicable to Advanced I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181

Note: *T_J = 100°C

Table 2-93 • **I/O Short Currents IOSH/IOSL (continued)**

	Drive Strength	IOSH (mA)*	IOSL (mA)*
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: *T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-95 • Schmitt Trigger Input Hysteresis, Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (Typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-94 • Short Current Event Duration before Failure

Temperature	Time before Failure
–55°C	>20 years
–40°C	>20 years
0°C	>20 years
25°C	>20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-96 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns*	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis	20 years (100°C)
HSTL/SSTL/GTL	No requirement	10 ns*	10 years (100°C)
LVDS/B-LVDS/M-LVDS/LVPECL	No requirement	10 ns*	10 years (100°C)

*Note: *The maximum input rise/fall time is related only to the noise induced into the input buffer trace. If the noise is low, the rise time and fall time of input buffers, when Schmitt trigger is disabled, can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

Table 2-97 • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/O banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	IOH	I_{OSH}	I_{OSL}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max mA[3]	µA[4]	µA[4]
Applicable to Pro I/O Banks												
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	15	15
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	15	15
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	15	15
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	15	15
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	15	15
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	15	15
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	15	15
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	15	15
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	15	15
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

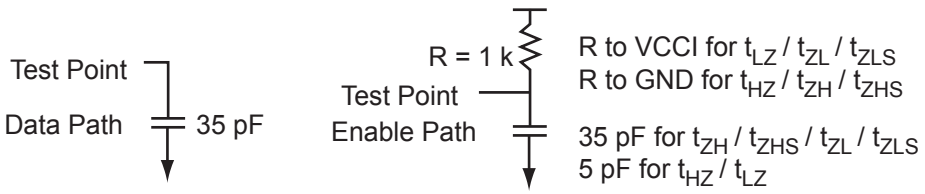


Figure 2-113 • AC Loading

Table 2-98 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

*Note: *Measuring point = V_{trip}. See Table 2-86 on page 2-163 for a complete table of trip points.*

Timing Characteristics

Table 2-99 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	11.61	0.05	1.27	1.65	0.44	11.82	9.55	2.84	2.58	14.18	11.90	ns
	–1	0.58	9.87	0.04	1.08	1.40	0.38	10.06	8.12	2.41	2.19	12.06	10.13	ns
	–2	0.51	8.67	0.03	0.95	1.23	0.33	8.83	7.13	2.12	1.92	10.59	8.89	ns
8 mA	Std.	0.68	8.29	0.05	1.27	1.65	0.44	8.45	6.79	3.20	3.23	10.80	9.15	ns
	–1	0.58	7.05	0.04	1.08	1.40	0.38	7.18	5.78	2.72	2.75	9.19	7.78	ns
	–2	0.51	6.19	0.03	0.95	1.23	0.33	6.31	5.07	2.39	2.41	8.07	6.83	ns
12 mA	Std.	0.68	6.35	0.05	1.27	1.65	0.44	6.47	5.29	3.45	3.66	8.83	7.65	ns
	–1	0.58	5.41	0.04	1.08	1.40	0.38	5.51	4.50	2.94	3.11	7.51	6.51	ns
	–2	0.51	4.75	0.03	0.95	1.23	0.33	4.83	3.95	2.58	2.73	6.59	5.71	ns
16 mA	Std.	0.68	5.93	0.05	1.27	1.65	0.44	6.04	4.98	3.50	3.77	8.39	7.34	ns
	–1	0.58	5.04	0.04	1.08	1.40	0.38	5.13	4.24	2.98	3.21	7.14	6.24	ns
	–2	0.51	4.42	0.03	0.95	1.23	0.33	4.51	3.72	2.62	2.82	6.27	5.48	ns
24 mA	Std.	0.68	5.53	0.05	1.27	1.65	0.44	5.63	4.95	3.57	4.18	7.99	7.31	ns
	–1	0.58	4.70	0.04	1.08	1.40	0.38	4.79	4.21	3.04	3.55	6.80	6.22	ns
	–2	0.51	4.13	0.03	0.95	1.23	0.33	4.21	3.70	2.67	3.12	5.97	5.46	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-100 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J =100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	8.31	0.05	1.27	1.65	0.44	8.47	7.07	2.84	2.73	10.82	9.43	ns
	–1	0.58	7.07	0.04	1.08	1.40	0.38	7.20	6.01	2.41	2.32	9.21	8.02	ns
	–2	0.51	6.21	0.03	0.95	1.23	0.33	6.32	5.28	2.12	2.04	8.08	7.04	s
8 mA	Std.	0.68	5.35	0.05	1.27	1.65	0.44	5.45	4.37	3.21	3.39	7.81	6.73	ns
	–1	0.58	4.55	0.04	1.08	1.40	0.38	4.64	3.72	2.73	2.88	6.64	5.72	ns
	–2	0.51	4.00	0.03	0.95	1.23	0.33	4.07	3.26	2.40	2.53	5.83	5.02	ns
12 mA	Std.	0.68	3.87	0.05	1.27	1.65	0.44	3.94	3.03	3.45	3.81	6.30	5.38	ns
	–1	0.58	3.29	0.04	1.08	1.40	0.38	3.35	2.57	2.94	3.24	5.36	4.58	ns
	–2	0.51	2.89	0.03	0.95	1.23	0.33	2.94	2.26	2.58	2.85	4.70	4.02	ns
16 mA	Std.	0.68	3.65	0.05	1.27	1.65	0.44	3.72	2.75	3.51	3.93	6.08	5.11	ns
	–1	0.58	3.11	0.04	1.08	1.40	0.38	3.16	2.34	2.99	3.34	5.17	4.34	ns
	–2	0.51	2.73	0.03	0.95	1.23	0.33	2.78	2.05	2.62	2.93	4.54	3.81	ns
24 mA	Std.	0.68	3.38	0.05	1.27	1.65	0.44	3.44	2.27	3.57	4.35	5.80	4.63	ns
	–1	0.58	2.88	0.04	1.08	1.40	0.38	2.93	1.93	3.04	3.70	4.94	3.94	ns
	–2	0.51	2.53	0.03	0.95	1.23	0.33	2.57	1.70	2.67	3.25	4.33	3.46	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-101 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	10.81	0.05	1.27	0.44	11.01	9.38	2.79	2.59	13.37	11.74	ns
	–1	0.58	9.20	0.04	1.08	0.38	9.37	7.98	2.37	2.20	11.38	9.99	ns
	–2	0.51	8.08	0.03	0.95	0.33	8.23	7.01	2.08	1.93	9.99	8.77	ns
8 mA	Std.	0.68	7.67	0.05	1.27	0.44	7.81	6.63	3.14	3.21	10.17	8.98	ns
	–1	0.58	6.53	0.04	1.08	0.38	6.65	5.64	2.67	2.73	8.65	7.64	ns
	–2	0.51	5.73	0.03	0.95	0.33	5.83	4.95	2.35	2.39	7.60	6.71	ns
12 mA	Std.	0.68	5.89	0.05	1.27	0.44	5.99	5.14	3.38	3.60	8.35	7.49	ns
	–1	0.58	5.01	0.04	1.08	0.38	5.10	4.37	2.88	3.06	7.10	6.38	ns
	–2	0.51	4.39	0.03	0.95	0.33	4.48	3.84	2.52	2.69	6.24	5.60	ns
16 mA	Std.	0.68	5.49	0.05	1.27	0.44	5.59	4.81	3.43	3.70	7.95	7.17	ns
	–1	0.58	4.67	0.04	1.08	0.38	4.76	4.09	2.92	3.15	6.76	6.10	ns
	–2	0.51	4.10	0.03	0.95	0.33	4.18	3.59	2.56	2.77	5.94	5.36	ns
24 mA	Std.	0.68	5.11	0.05	1.27	0.44	5.21	4.79	3.50	4.10	7.57	7.15	ns
	–1	0.58	4.35	0.04	1.08	0.38	4.43	4.08	2.98	3.48	6.44	6.08	ns
	–2	0.51	3.82	0.03	0.95	0.33	3.89	3.58	2.61	3.06	5.65	5.34	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-102 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	8.07	0.05	1.27	0.44	8.22	6.95	2.79	2.76	10.58	9.31	ns
	–1	0.58	6.87	0.04	1.08	0.38	6.99	5.91	2.38	2.34	9.00	7.92	ns
	–2	0.51	6.03	0.03	0.95	0.33	6.14	5.19	2.09	2.06	7.90	6.95	ns
8 mA	Std.	0.68	5.17	0.05	1.27	0.44	5.27	4.29	3.15	3.38	7.63	6.65	ns
	–1	0.58	4.40	0.04	1.08	0.38	4.48	3.65	2.68	2.87	6.49	5.66	ns
	–2	0.51	3.86	0.03	0.95	0.33	3.94	3.20	2.35	2.52	5.70	4.97	ns
12 mA	Std.	0.68	3.73	0.05	1.27	0.44	3.79	2.98	3.39	3.78	6.15	5.34	ns
	–1	0.58	3.17	0.04	1.08	0.38	3.23	2.53	2.88	3.21	5.23	4.54	ns
	–2	0.51	2.78	0.03	0.95	0.33	2.83	2.22	2.53	2.82	4.59	3.99	ns
16 mA	Std.	0.68	3.51	0.05	1.27	0.44	3.58	2.70	3.44	3.88	5.94	5.06	ns
	–1	0.58	2.99	0.04	1.08	0.38	3.04	2.30	2.93	3.30	5.05	4.31	ns
	–2	0.51	2.62	0.03	0.95	0.33	2.67	2.02	2.57	2.90	4.43	3.78	ns
24 mA	Std.	0.68	3.24	0.05	1.27	0.44	3.30	2.23	3.51	4.28	5.66	4.59	ns
	–1	0.58	2.76	0.04	1.08	0.38	2.81	1.90	2.98	3.64	4.82	3.91	ns
	–2	0.51	2.42	0.03	0.95	0.33	2.47	1.67	2.62	3.20	4.23	3.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V–tolerant input buffer and push-pull output buffer.

Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
Applicable to Pro I/O Banks												
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	10	10

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

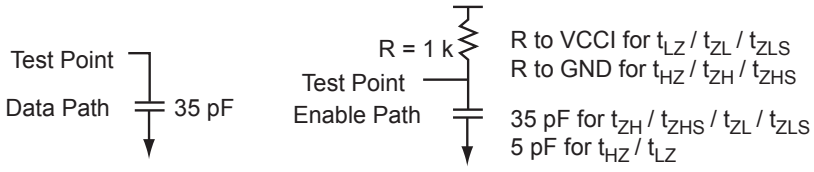


***Figure 2-114* • AC Loading**

***Table 2-103* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

*Note: *Measuring point = V_{trip}. See Table 2-86 on page 2-163 for a complete table of trip points.*

Timing Characteristics

Table 2-104 • 2.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	12.66	0.05	1.59	1.75	0.44	12.89	12.24	2.87	2.32	15.25	14.60	ns
	–1	0.58	10.77	0.04	1.36	1.49	0.38	10.97	10.42	2.44	1.97	12.97	12.42	ns
	–2	0.51	9.45	0.03	1.19	1.31	0.33	9.63	9.14	2.14	1.73	11.39	10.90	ns
8 mA	Std.	0.68	9.21	0.05	1.59	1.75	0.44	9.38	8.45	3.27	3.09	11.74	10.81	ns
	–1	0.58	7.83	0.04	1.36	1.49	0.38	7.98	7.19	2.78	2.63	9.98	9.19	ns
	–2	0.51	6.88	0.03	1.19	1.31	0.33	7.00	6.31	2.44	2.31	8.76	8.07	ns
12 mA	Std.	0.68	7.14	0.05	1.59	1.75	0.44	7.28	6.44	3.55	3.58	9.63	8.80	ns
	–1	0.58	6.08	0.04	1.36	1.49	0.38	6.19	5.48	3.02	3.04	8.20	7.48	ns
	–2	0.51	5.33	0.03	1.19	1.31	0.33	5.43	4.81	2.65	2.67	7.19	6.57	ns
16 mA	Std.	0.68	6.65	0.05	1.59	1.75	0.44	6.77	6.04	3.61	3.71	9.13	8.40	ns
	–1	0.58	5.66	0.04	1.36	1.49	0.38	5.76	5.14	3.07	3.16	7.77	7.14	ns
	–2	0.51	4.97	0.03	1.19	1.31	0.33	5.06	4.51	2.69	2.77	6.82	6.27	ns
24 mA	Std.	0.68	6.25	0.05	1.59	1.75	0.44	6.37	6.02	3.69	4.22	8.73	8.37	ns
	–1	0.58	5.32	0.04	1.36	1.49	0.38	5.42	5.12	3.14	3.59	7.43	7.12	ns
	–2	0.51	4.67	0.03	1.19	1.31	0.33	4.76	4.49	2.75	3.15	6.52	6.25	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-105 • 2.5 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	9.30	0.05	1.59	1.75	0.44	8.57	9.30	2.87	2.41	10.93	11.65	ns
	–1	0.58	7.91	0.04	1.36	1.49	0.38	7.29	7.91	2.44	2.05	9.30	9.91	ns
	–2	0.51	6.94	0.03	1.19	1.31	0.33	6.40	6.94	2.14	1.80	8.16	8.70	ns
8 mA	Std.	0.68	5.56	0.05	1.59	1.75	0.44	5.56	5.56	3.27	3.19	7.91	7.92	ns
	–1	0.58	4.73	0.04	1.36	1.49	0.38	4.73	4.73	2.78	2.72	6.73	6.73	ns
	–2	0.51	4.15	0.03	1.19	1.31	0.33	4.15	4.15	2.44	2.38	5.91	5.91	ns
12 mA	Std.	0.68	3.95	0.05	1.59	1.75	0.44	4.02	3.68	3.55	3.69	6.38	6.04	ns
	–1	0.58	3.36	0.04	1.36	1.49	0.38	3.42	3.13	3.02	3.14	5.43	5.14	ns
	–2	0.51	2.95	0.03	1.19	1.31	0.33	3.00	2.75	2.65	2.75	4.76	4.51	ns
16 mA	Std.	0.68	3.72	0.05	1.59	1.75	0.44	3.79	3.29	3.61	3.82	6.15	5.65	ns
	–1	0.58	3.16	0.04	1.36	1.49	0.38	3.22	2.80	3.07	3.25	5.23	4.80	ns
	–2	0.51	2.78	0.03	1.19	1.31	0.33	2.83	2.46	2.69	2.85	4.59	4.22	ns
24 mA	Std.	0.68	3.44	0.05	1.59	1.75	0.44	3.50	2.62	3.69	4.33	5.86	4.98	ns
	–1	0.58	2.93	0.04	1.36	1.49	0.38	2.98	2.23	3.14	3.68	4.99	4.23	ns
	–2	0.51	2.57	0.03	1.19	1.31	0.33	2.62	1.95	2.75	3.23	4.38	3.72	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-106 • 2.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	12.02	0.05	1.38	0.44	11.83	12.02	2.82	2.33	14.19	14.38	ns
	–1	0.58	10.22	0.04	1.18	0.38	10.06	10.22	2.40	1.98	12.07	12.23	ns
	–2	0.51	8.97	0.03	1.03	0.33	8.83	8.97	2.11	1.74	10.59	10.74	ns
8 mA	Std.	0.68	8.39	0.05	1.38	0.44	8.55	8.24	3.22	3.05	10.91	10.60	ns
	–1	0.58	7.14	0.04	1.18	0.38	7.27	7.01	2.74	2.59	9.28	9.02	ns
	–2	0.51	6.27	0.03	1.03	0.33	6.38	6.15	2.40	2.28	8.15	7.91	ns
12 mA	Std.	0.68	6.52	0.05	1.38	0.44	6.64	6.24	3.48	3.50	8.99	8.60	ns
	–1	0.58	5.54	0.04	1.18	0.38	5.65	5.31	2.96	2.98	7.65	7.31	ns
	–2	0.51	4.87	0.03	1.03	0.33	4.96	4.66	2.60	2.62	6.72	6.42	ns
16 mA	Std.	0.68	6.08	0.05	1.38	0.44	6.19	5.83	3.54	3.63	8.55	8.18	ns
	–1	0.58	5.17	0.04	1.18	0.38	5.27	4.96	3.01	3.08	7.27	6.96	ns
	–2	0.51	4.54	0.03	1.03	0.33	4.62	4.35	2.65	2.71	6.38	6.11	ns
24 mA	Std.	0.68	5.81	0.05	1.38	0.44	5.80	5.81	3.62	4.08	8.16	8.16	ns
	–1	0.58	4.94	0.04	1.18	0.38	4.94	4.94	3.08	3.47	6.94	6.95	ns
	–2	0.51	4.34	0.03	1.03	0.33	4.33	4.34	2.70	3.05	6.09	6.10	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-107 • 2.5 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	9.14	0.05	1.38	0.44	8.26	9.14	2.82	2.43	10.62	11.49	ns
	–1	0.58	7.77	0.04	1.18	0.38	7.03	7.77	2.40	2.07	9.03	9.78	ns
	–2	0.51	6.82	0.03	1.03	0.33	6.17	6.82	2.11	1.81	7.93	8.58	ns
8 mA	Std.	0.68	5.45	0.05	1.38	0.44	5.31	5.45	3.22	3.16	7.67	7.81	ns
	–1	0.58	4.63	0.04	1.18	0.38	4.52	4.63	2.74	2.69	6.52	6.64	ns
	–2	0.51	4.07	0.03	1.03	0.33	3.97	4.07	2.40	2.36	5.73	5.83	ns
12 mA	Std.	0.68	3.75	0.05	1.38	0.44	3.82	3.62	3.48	3.62	6.18	5.98	ns
	–1	0.58	3.19	0.04	1.18	0.38	3.25	3.08	2.95	3.08	5.26	5.09	ns
	–2	0.51	2.80	0.03	1.03	0.33	2.86	2.70	2.60	2.71	4.62	4.46	ns
16 mA	Std.	0.68	3.53	0.05	1.38	0.44	3.60	3.23	3.54	3.74	5.96	5.59	ns
	–1	0.58	3.01	0.04	1.18	0.38	3.06	2.75	3.02	3.18	5.07	4.75	ns
	–2	0.51	2.64	0.03	1.03	0.33	2.69	2.41	2.65	2.79	4.45	4.17	ns
24 mA	Std.	0.68	3.26	0.05	1.38	0.44	3.32	2.58	3.62	4.22	5.68	4.93	ns
	–1	0.58	2.77	0.04	1.18	0.38	2.82	2.19	3.08	3.59	4.83	4.20	ns
	–2	0.51	2.43	0.03	1.03	0.33	2.48	1.92	2.71	3.15	4.24	3.68	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and push-pull output buffer.

Table 2-108 • Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
Applicable to Pro I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	11	9	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	22	17	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	44	35	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	51	45	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12	74	91	15	15
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	16	16	74	91	15	15
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	11	9	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	22	17	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	6	6	44	35	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8	51	45	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12	74	91	15	15
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	16	16	74	91	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

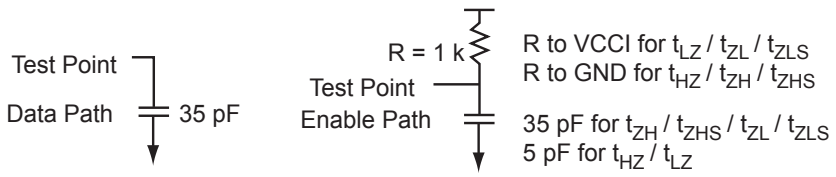


Figure 2-115 • AC Loading

Table 2-109 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input Low (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

*Note: *Measuring point = V_{trip}. See Table 2-86 on page 2-163 for a complete table of trip points.*

Timing Characteristics

Table 2-110 • 1.8 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	16.70	0.05	1.53	2.01	0.44	16.50	16.70	2.93	1.67	18.86	19.06	ns
	–1	0.58	14.21	0.04	1.30	1.71	0.38	14.04	14.21	2.50	1.42	16.05	16.21	ns
	–2	0.51	12.47	0.03	1.14	1.50	0.33	12.32	12.47	2.19	1.25	14.09	14.23	ns
4 mA	Std.	0.68	12.01	0.05	1.53	2.01	0.44	12.24	11.34	3.43	2.92	14.59	13.70	ns
	–1	0.58	10.22	0.04	1.30	1.71	0.38	10.41	9.65	2.92	2.49	12.41	11.66	ns
	–2	0.51	8.97	0.03	1.14	1.50	0.33	9.14	8.47	2.56	2.18	10.90	10.23	ns
6 mA	Std.	0.68	9.46	0.05	1.53	2.01	0.44	9.54	8.54	3.76	3.54	11.99	10.90	ns
	–1	0.58	8.05	0.04	1.30	1.71	0.38	8.20	7.26	3.20	3.01	10.20	9.27	ns
	–2	0.51	7.06	0.03	1.14	1.50	0.33	7.20	6.38	2.81	2.64	8.96	8.14	ns
8 mA	Std.	0.68	8.81	0.05	1.53	2.01	0.44	8.97	8.00	3.84	3.71	11.33	10.36	ns
	–1	0.58	7.49	0.04	1.30	1.71	0.38	7.63	6.80	3.27	3.16	9.64	8.81	ns
	–2	0.51	6.58	0.03	1.14	1.50	0.33	6.70	5.97	2.87	2.77	8.46	7.73	ns
12 mA	Std.	0.68	8.37	0.05	1.53	2.01	0.44	8.53	7.97	3.95	4.33‘	10.89	10.33	ns
	–1	0.58	7.12	0.04	1.30	1.71	0.38	7.25	6.78	3.36	3.68	9.26	8.79	ns
	–2	0.51	6.25	0.03	1.14	1.50	0.33	6.37	5.95	2.85	3.23	8.13	7.71	ns
16 mA	Std.	0.68	8.37	0.05	1.53	2.01	0.44	8.53	7.97	3.95	4.33	10.89	10.33	ns
	–1	0.58	7.12	0.04	1.30	1.71	0.38	7.25	6.78	3.36	3.68	9.26	8.79	ns
	–2	0.51	6.25	0.03	1.14	1.50	0.33	6.37	5.95	2.95	3.23	8.13	7.71	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-111 • 1.8 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J =100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	12.76	0.05	1.53	2.01	0.44	10.11	12.76	2.93	1.73	12.47	15.12	ns
	–1	0.58	10.86	0.04	1.30	1.71	0.38	8.60	10.86	2.50	1.47	10.61	12.86	ns
	–2	0.51	9.53	0.03	1.14	1.50	0.33	7.55	9.53	2.19	1.29	9.31	11.29	ns
4 mA	Std.	0.68	7.44	0.05	1.53	2.01	0.44	6.54	7.44	3.43	3.02	8.90	9.79	ns
	–1	0.58	6.33	0.04	1.30	1.71	0.38	5.56	6.33	2.91	2.57	7.57	8.33	ns
	–2	0.51	5.55	0.03	1.14	1.50	0.33	4.88	5.55	2.56	2.26	6.64	7.31	ns
6 mA	Std.	0.68	4.77	0.05	1.53	2.01	0.44	4.71	4.77	3.76	3.66	7.07	7.13	ns
	–1	0.58	4.06	0.04	1.30	1.71	0.38	4.01	4.06	3.20	3.11	6.01	6.06	ns
	–2	0.51	3.56	0.03	1.14	1.50	0.33	3.52	3.56	2.81	2.73	5.28	5.32	ns
8 mA	Std.	0.68	4.35	0.05	1.53	2.01	0.44	4.43	4.21	3.83	3.82	6.79	6.57	ns
	–1	0.58	3.70	0.04	1.30	1.71	0.38	3.77	3.58	3.26	3.25	5.77	5.59	ns
	–2	0.51	3.25	0.03	1.14	1.50	0.33	3.31	3.14	2.86	2.85	5.07	4.91	ns
12 mA	Std.	0.68	4.00	0.05	1.53	2.01	0.44	3.80	3.21	3.90	4.30	6.15	5.57	ns
	–1	0.58	3.41	0.04	1.30	1.71	0.38	3.23	2.73	3.32	3.66	5.23	4.73	ns
	–2	0.51	2.99	0.03	1.14	1.50	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns
16 mA	Std.	0.68	4.00	0.035	1.53	2.01	0.44	3.80	3.21	3.90	4.30	6.15	5.57	ns
	–1	0.58	3.41	0.04	1.30	1.71	0.38	3.23	2.73	3.32	3.66	5.23	4.73	ns
	–2	0.51	2.99	0.03	1.14	1.50	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-112 • 1.8 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	16.70	0.05	1.38	0.44	14.88	16.38	2.93	1.69	17.24	18.73	ns
	–1	0.58	14.21	0.04	1.18	0.38	12.66	13.93	2.49	1.44	14.67	15.94	ns
	–2	0.51	12.47	0.03	1.03	0.33	11.11	12.23	2.19	1.26	12.87	13.99	ns
4 mA	Std.	0.68	12.01	0.05	1.38	0.44	10.98	11.05	3.40	2.88	13.34	13.41	ns
	–1	0.58	10.22	0.04	1.18	0.38	9.34	9.40	2.90	2.45	11.34	11.40	ns
	–2	0.51	8.97	0.03	1.03	0.33	8.20	8.25	2.54	2.15	9.96	10.01	ns
6 mA	Std.	0.68	9.46	0.05	1.38	0.44	8.65	8.27	3.73	3.45	11.00	10.63	ns
	–1	0.58	8.05	004	1.18	0.38	7.35	7.03	3.17	2.94	9.36	9.04	ns
	–2	0.51	7.06	0.03	1.03	0.33	6.46	6.17	2.78	2.58	8.22	7.94	ns
8 mA	Std.	0.68	7.91	0.05	1.38	0.44	8.06	7.70	3.80	3.60	10.42	10.05	ns
	–1	0.58	6.73	0.04	1.18	0.38	6.85	6.55	3.23	3.06	8.86	8.55	ns
	–2	0.51	5.91	0.03	1.03	0.33	6.02	5.75	2.84	2.69	7.78	7.51	ns
12 mA	Std.	0.68	7.69	0.05	1.38	0.44	7.63	7.69	3.91	4.17	9.99	10.05	ns
	–1	0.58	6.54	0.04	1.18	0.38	6.49	6.54	3.32	3.54	8.50	8.55	ns
	–2	0.51	5.74	0.03	1.03	0.33	5.70	5.74	2.92	3.11	7.46	7.50	ns
16 mA	Std.	0.68	7.69	0.05	1.38	0.44	7.63	7.69	3.91	4.17	9.99	10.05	ns
	–1	0.58	6.54	0.04	1.18	0.38	6.49	6.54	3.32	3.54	8.50	8.55	ns
	–2	0.51	5.74	0.03	1.03	0.33	5.70	5.74	2.92	3.11	7.46	7.50	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-113 • 1.8 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	12.51	0.05	1.53	0.44	9.63	12.51	2.92	1.75	11.99	14.87	ns
	–1	0.58	10.64	0.04	1.30	0.38	8.19	10.64	2.49	1.49	10.20	12.65	ns
	–2	0.51	9.34	0.03	1.14	0.33	7.19	9.34	2.18	1.30	8.96	11.10	ns
4 mA	Std.	0.68	7.44	0.05	1.53	0.44	6.18	7.29	3.40	2.99	8.54	9.65	ns
	–1	0.58	6.33	0.04	1.30	0.38	5.26	6.20	2.89	2.55	7.26	8.21	ns
	–2	0.51	5.55	0.03	1.14	0.33	4.62	5.45	2.54	2.23	6.38	7.21	ns
6 mA	Std.	0.68	4.77	0.05	1.53	0.44	4.41	4.69	3.72	3.57	6.77	7.05	ns
	–1	0.58	4.06	0.04	1.30	0.38	3.75	3.99	3.17	3.03	5.76	6.00	ns
	–2	0.51	3.56	0.03	1.14	0.33	3.29	3.50	2.78	2.66	5.05	5.26	ns
8 mA	Std.	0.68	4.35	0.05	1.53	0.44	4.14	4.14	3.80	3.71	6.50	6.50	ns
	–1	0.58	3.70	0.04	1.30	0.38	3.52	3.52	3.23	3.16	5.53	5.53	ns
	–2	0.51	3.25	0.03	1.14	0.33	3.09	3.09	2.83	2.77	4.85	4.85	ns
12 mA	Std.	0.68	4.00	0.05	1.53	0.44	3.80	3.21	3.90	4.30	6.15	5.57	ns
	–1	0.58	3.41	0.04	1.30	0.38	3.23	2.73	3.32	3.66	5.23	4.73	ns
	–2	0.51	2.99	0.03	1.14	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns
16 mA	Std.	0.68	4.00	0.05	1.53	0.44	3.80	3.21	3.90	4.30	6.15	5.57	ns
	–1	0.58	3.41	0.04	1.30	0.38	3.23	2.73	3.32	3.66	5.23	4.73	ns
	–2	0.51	2.99	0.03	1.14	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and push-pull output buffer.

Table 2-114 • Minimum and Maximum DC Input and Output Levels

1.5 V LVCMOS	VIL		V_{IH}		VOL	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
Applicable to Pro I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	55	66	15	15
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	39	32	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	55	66	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	55	66	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

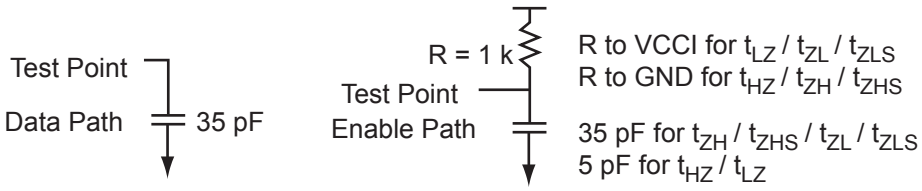


Figure 2-116 • AC Loading

Table 2-115 • 1.5 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	35

*Note: *Measuring point = Vtrip. See Table 2-86 on page 2-163 for a complete table of trip points.*

Timing Characteristics

Table 2-116 • 1.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	14.88	0.05	1.52	2.26	0.44	15.15	13.85	3.59	2.83	17.51	16.21	ns
	–1	0.58	12.66	0.04	1.29	1.92	0.38	12.89	11.78	3.05	2.40	14.90	13.79	ns
	–2	0.51	11.11	0.03	1.13	1.69	0.33	11.32	10.34	2.68	2.11	13.08	12.11	ns
4 mA	Std.	0.68	11.84	0.05	1.52	2.26	0.44	12.06	10.40	3.97	3.54	14.42	12.76	ns
	–1	0.58	10.07	0.04	1.29	1.92	0.38	10.26	8.85	3.38	3.01	12.27	10.86	ns
	–2	0.51	8.84	0.03	1.13	1.69	0.33	9.01	7.77	2.97	2.64	10.77	9.53	ns
6 mA	Std.	0.68	11.02	0.05	1.52	2.26	0.44	11.23	9.75	4.05	3.74	13.58	12.10	ns
	–1	0.58	9.38	0.04	1.29	1.92	0.38	9.55	8.29	3.45	3.18	11.56	10.30	ns
	–2	0.51	8.23	0.03	1.13	1.69	0.33	8.38	7.28	3.03	2.80	10.14	9.04	ns
8 mA	Std.	0.68	10.57	0.05	1.52	2.26	0.44	10.76	9.73	4.19	4.45	13.12	12.09	ns
	–1	0.58	8.99	0.04	1.29	1.92	0.38	9.15	8.28	3.56	3.78	11.16	10.29	ns
	–2	0.51	7.89	0.03	1.13	1.69	0.33	8.04	7.27	3.13	3.32	9.80	9.03	ns
12 mA	Std.	0.68	9.39	0.05	1.52	2.26	0.44	9.57	9.38	4.17	4.27	11.93	11.74	ns
	–1	0.58	2.99	0.04	1.29	1.92	0.38	8.14	7.98	3.55	3.63	10.14	9.98	ns
	–2	0.51	7.01	0.03	1.13	1.69	0.33	7.14	7.00	3.11	3.19	8.91	8.76	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-117 • 1.5 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	8.82	0.05	1.52	2.26	0.44	7.20	8.82	3.57	2.92	9.55	11.18	ns
	–1	0.58	7.50	0.04	1.29	1.92	0.38	6.12	7.50	3.04	2.48	8.13	9.51	ns
	–2	0.51	6.59	0.03	1.13	1.69	0.33	5.37	6.59	2.67	2.18	7.13	8.35	ns
4 mA	Std.	0.68	5.60	0.05	1.52	2.26	0.44	5.11	5.60	3.94	3.59	7.47	7.96	ns
	–1	0.58	4.77	0.04	1.29	1.92	0.38	4.35	4.77	3.36	3.05	6.36	6.77	ns
	–2	0.51	4.18	0.03	1.13	1.69	0.33	3.82	4.18	2.95	2.68	5.58	5.95	ns
6 mA	Std.	0.68	5.07	0.05	1.52	2.26	0.44	4.80	4.92	4.03	3.76	7.15	7.28	ns
	–1	0.58	4.31	0.04	1.29	1.92	0.38	4.08	4.19	3.43	3.20	6.09	6.19	ns
	–2	0.51	3.78	0.03	1.13	1.69	0.33	3.58	3.68	3.01	2.81	5.34	5.44	ns
8 mA	Std.	0.68	4.66	0.05	1.52	2.26	0.44	4.38	3.77	4.16	4.43	6.74	6.13	ns
	–1	0.58	3.96	0.04	1.29	1.92	0.38	3.73	3.21	3.54	3.77	5.73	5.21	ns
	–2	0.51	3.48	0.03	1.13	1.69	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns
12 mA	Std.	0.68	4.30	0.05	1.52	2.26	0.44	4.38	3.77	4.16	4.43	6.74	6.13	ns
	–1	0.58	3.66	0.04	1.29	1.92	0.38	3.73	3.21	3.54	3.77	5.73	5.21	ns
	–2	0.51	3.21	0.03	1.13	1.69	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-118 • 1.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	13.48	0.05	1.38	0.44	13.51	13.48	3.58	2.79	15.87	15.84	ns
	–1	0.58	11.47	0.04	1.18	0.38	11.49	11.47	3.05	2.37	13.50	13.47	ns
	–2	0.51	10.07	0.03	1.03	0.33	10.09	10.07	2.68	2.08	11.85	11.83	ns
4 mA	Std.	0.68	10.55	0.05	1.38	0.44	10.75	10.07	3.95	3.45	13.11	12.43	ns
	–1	0.58	8.98	0.04	1.18	0.38	9.14	8.56	3.36	2.93	11.15	10.57	ns
	–2	0.51	7.88	0.03	1.03	0.33	8.03	7.52	2.95	2.58	9.79	9.28	ns
6 mA	Std.	0.68	9.84	0.05	1.38	0.44	10.03	9.38	4.04	3.62	12.38	11.73	ns
	–1	0.58	8.37	0.04	1.18	0.38	8.53	7.98	3.44	3.08	10.53	9.98	ns
	–2	0.51	7.35	0.03	1.03	0.33	7.49	7.00	3.02	2.70	9.25	8.76	ns
8 mA	Std.	0.68	9.39	0.05	1.38	0.44	9.57	9.38	4.17	4.27	11.93	11.74	ns
	–1	0.58	7.99	0.04	1.18	0.38	8.14	7.98	3.55	3.63	10.14	9.98	ns
	–2	0.51	7.01	0.03	1.03	0.33	7.14	7.00	3.11	3.19	8.91	8.76	ns
12 mA	Std.	0.68	9.39	0.05	1.38	0.44	9.57	9.38	4.17	4.27	11.93	11.74	ns
	–1	0.58	7.99	0.04	1.18	0.38	8.14	7.98	3.55	3.63	10.14	9.98	ns
	–2	0.51	7.01	0.03	1.03	0.33	7.14	7.00	3.11	3.19	8.91	8.76	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-119 • 1.5 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	9.00	0.05	1.79	0.44	7.20	8.82	3.57	2.92	9.55	11.18	ns
	–1	0.58	7.65	0.04	1.52	0.38	6.12	7.50	3.04	2.48	8.13	9.51	ns
	–2	0.51	6.72	0.03	1.34	0.33	5.37	6.59	2.67	2.18	7.13	8.35	ns
4 mA	Std.	0.68	5.71	0.05	1.79	0.44	5.11	5.60	3.94	3.59	7.47	7.96	ns
	–1	0.58	4.85	0.04	1.52	0.38	4.35	4.77	3.36	3.05	6.36	6.77	ns
	–2	0.51	4.26	0.03	1.34	0.33	3.82	4.18	2.95	2.68	5.58	5.95	ns
6 mA	Std.	0.68	5.07	0.05	1.79	0.44	4.80	4.92	4.03	3.76	7.15	7.28	ns
	–1	0.58	4.31	0.04	1.52	0.38	4.08	4.19	3.43	3.20	6.09	6.19	ns
	–2	0.51	3.78	0.03	1.34	0.33	3.58	3.68	3.01	2.81	5.34	5.44	ns
8 mA	Std.	0.68	4.66	0.05	1.79	0.44	4.38	3.77	4.16	4.43	6.74	6.13	ns
	–1	0.58	3.96	0.04	1.52	0.38	3.73	3.21	3.54	3.77	5.73	5.21	ns
	–2	0.51	3.48	0.03	1.34	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns
12 mA	Std.	0.68	4.66	0.05	1.79	0.44	4.38	3.77	4.16	4.43	6.74	6.13	ns
	–1	0.58	3.96	0.04	1.52	0.38	3.73	3.21	3.54	3.77	5.73	5.21	ns
	–2	0.51	3.48	0.03	1.34	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

3.3 V PCI, 3.3 V PCI-X

The Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-120 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
Per PCI specification	Per PCI curves										10	10

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in Figure 2-117.

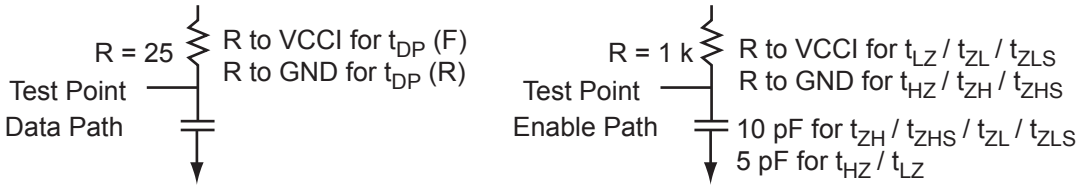


Figure 2-117 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the data path; Actel loading for tristate is described in Table 2-121.

Table 2-121 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCC_I for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$	–	10

*Note: *Measuring point = V_{trip}. See Table 2-86 on page 2-163 for a complete table of trip points.*

Timing Characteristics

Table 2-122 • 3.3 V PCI/PCI-X, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 3.0 V
Applicable to Pro I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.96	0.05	1.11	1.76	0.44	3.01	2.10	3.45	3.81	5.37	4.46	ns
–1	0.58	2.52	0.04	0.94	1.50	0.38	2.56	1.79	2.94	3.24	4.57	3.80	ns
–2	0.51	2.21	0.03	0.83	1.32	0.33	2.25	1.57	2.58	2.85	4.01	3.33	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-123 • 3.3 V PCI/PCI-X, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 3.0 V
Applicable to Advanced I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.83	0.05	0.91	0.44	2.88	2.06	3.39	3.78	5.24	4.42	ns
–1	0.58	2.40	0.04	0.77	0.38	2.45	1.75	2.88	3.21	4.45	3.76	ns
–2	0.51	2.11	0.03	0.68	0.33	2.15	1.54	2.53	2.82	3.91	3.30	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Voltage Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-124 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [4]	II_H [5]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
25 mA[3]	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	25	25	181	268	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*
4. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL*
5. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

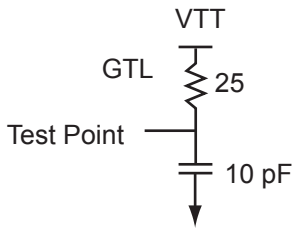


Figure 2-118 • AC Loading

Table 2-125 • 3.3 V GTL AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

*Note: *Measuring point* = Vtrip. *See Table 2-77 on page 2-150 for a complete table of trip points.*

Timing Characteristics

Table 2-126 • 3.3 V GTL
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 3.0 V, VREF = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.19	0.05	3.09	0.44	2.15	2.19			4.51	4.55	ns
–1	0.58	1.86	0.04	2.63	0.38	1.83	1.86			3.83	3.87	ns
–2	0.51	1.63	0.03	2.31	0.33	1.60	1.63			3.36	3.40	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-127 • Minimum and Maximum DC Input and Output Levels

2.5 GTL	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [4]	I_{IH} [5]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [1]	Max. mA [1]	µA [2]	µA [2]
25 mA [3]	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	25	25	124	169	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*
4. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
5. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

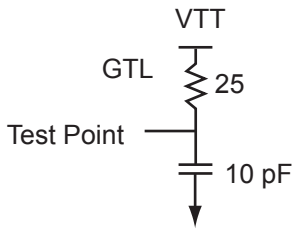


Figure 2-119 • AC Loading

Table 2-128 • 2.5 GTL AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

*Note: *Measuring point = Vtrip. See Table 2-77 on page 2-150 for a complete table of trip points.*

Timing Characteristics

Table 2-129 • 2.5 V GTL
Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.24	0.05	2.59	0.44	2.28	2.24			4.64	4.60	ns
–1	0.58	1.91	0.04	2.20	0.38	1.94	1.91			3.95	3.91	ns
–2	0.51	1.68	0.03	1.93	0.33	1.70	1.68			3.46	3.44	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-130 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL+	VIL		VIH		V_{OL}	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[3]	I_{IH}[4]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[2]	µA[2]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	181	268	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

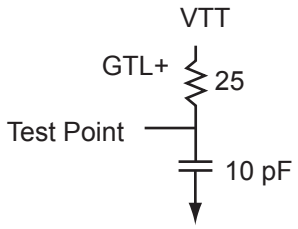


Figure 2-120 • AC Loading

Table 2-131 • 3.3 V GTL+ AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = V_{trip}. See Table 2-77 on page 2-150 for a complete table of trip points.*

Timing Characteristics

Table 2-132 • 3.3 V GTL+
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.17	0.05	1.68	0.44	2.21	2.17			4.57	4.53	ns
–1	0.58	1.84	0.04	1.43	0.38	1.88	1.84			3.88	3.85	ns
–2	0.51	1.62	0.03	1.25	0.33	1.65	1.62			3.41	3.38	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-133 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
33 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33	124	169	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

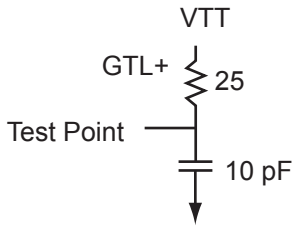


Figure 2-121 • AC Loading

Table 2-134 • 2.5 V GTL+ AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-77 on page 2-150 for a complete table of trip points.*

Timing Characteristics

Table 2-135 • 2.5 V GTL+
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.33	0.05	1.60	0.44	2.37	2.21			4.73	4.57	ns
–1	0.58	1.98	0.04	1.36	0.38	2.02	1.88			4.02	3.89	ns
–2	0.51	1.74	0.03	1.19	0.33	1.77	1.65			3.53	3.41	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-136 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
8 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8	39	32	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

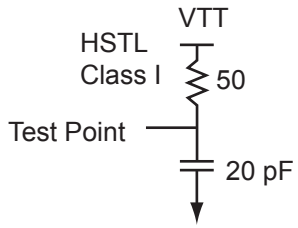


Figure 2-122 • AC Loading

Table 2-137 • HSTL Class I AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note: *Measuring point = V*trip. *See Table 2-77 on page 2-150 for a complete table of trip points.*

Timing Characteristics

Table 2-138 • HSTL Class I
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	3.25	0.05	2.24	0.44	3.41	3.31			5.77	5.67	ns
–1	0.58	2.85	0.04	1.91	0.38	2.90	2.82			4.91	4.83	ns
–2	0.51	2.50	0.03	1.67	0.33	2.55	2.48			4.31	4.24	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-139 • Minimum and Maximum DC Input and Output Levels

HSTL Class II	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}[1]	II_H[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max mA[3]	µA[4]	µA[4]
15 mA[3]	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15	55	66	15	15

Note:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Output drive strength is below JEDEC specification.*

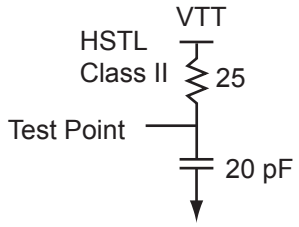


Figure 2-123 • AC Loading

Table 2-140 • HSTL Class II AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note: *Measuring point = Vtrip. See Table 2-77 on page 2-150 for a complete table of trip points.*

Timing Characteristics

Table 2-141 • HSTL Class II
Extended Temperature Range Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	3.19	0.05	2.24	0.44	3.25	2.86			5.61	5.22	ns
–1	0.58	2.71	0.04	1.91	0.38	2.76	2.43			4.77	4.44	ns
–2	0.51	2.38	0.03	1.67	0.33	2.43	2.14			4.19	3.90	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-142 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
17 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	17	17	87	83	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

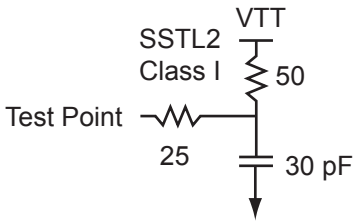


Figure 2-124 • AC Loading

Table 2-143 • SSTL2 Class I AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-77 on page 2-150 for a complete table of trip points.*

Timing Characteristics

Table 2-144 • SSTL 2 Class I
Extended Temperature Range Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.24	0.05	1.41	0.44	2.28	1.95			4.64	4.31	ns
–1	0.58	1.91	0.04	1.20	0.38	1.94	1.66			3.95	3.66	ns
–2	0.51	1.68	0.03	1.05	0.33	1.71	1.45			3.47	3.22	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-145 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max mA [3]	Max. mA [3]	µA [4]	µA [4]
21 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	21	21	124	169	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

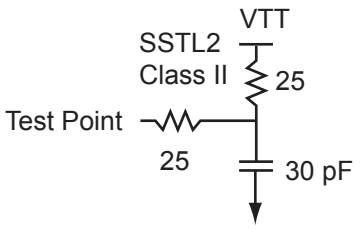


Figure 2-125 • AC Loading

SSTL2 Class II

Table 2-146 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = V_{trip}. See Table 2-77 on page 2-150 for a complete table of trip points.*

Timing Characteristics

Table 2-147 • SSTL 2 Class II
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.29	0.05	1.41	0.44	2.33	1.87			4.69	4.22	ns
–1	0.58	1.94	0.04	1.20	0.38	1.98	1.59			3.99	3.59	ns
–2	0.51	1.71	0.03	1.05	0.33	1.74	1.39			3.50	3.15	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-148 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class I	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	II_H [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
16 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	16	16	54	51	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

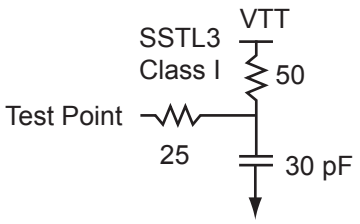


Figure 2-126 • AC Loading

SSTL3 Class I

Table 2-149 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = Vtrip. See Table 2-77 on page 2-150 for a complete table of trip points.*

Timing Characteristics

Table 2-150 • SSTL3 Class I
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.43	0.05	1.32	0.44	2.48	1.94			4.84	4.29	ns
–1	0.58	2.07	0.04	1.12	0.38	2.11	1.65			4.11	3.65	ns
–2	0.51	1.82	0.03	0.99	0.33	1.85	1.45			3.61	3.21	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-151 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} [1]	II_H [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
24 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	24	24	109	103	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

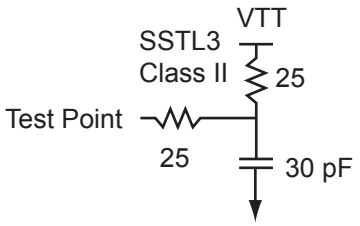


Figure 2-127 • AC Loading

Table 2-152 • SSTL3 Class II AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = Vtrip. See Table 2-77 on page 2-150 for a complete table of trip points.*

Timing Characteristics

Table 2-153 • SSTL3- Class II
Extended Temperature Range Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.18	0.05	1.32	0.44	2.22	1.76			4.58	4.12	ns
–1	0.58	1.85	0.04	1.12	0.38	1.89	1.50			3.89	3.51	ns
–2	0.51	1.63	0.03	0.99	0.33	1.66	1.32			3.42	3.08	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Differential I/O Characteristics

Configuration of the I/O modules as a differential pair is handled by the Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-128. The building blocks of the LVDS transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

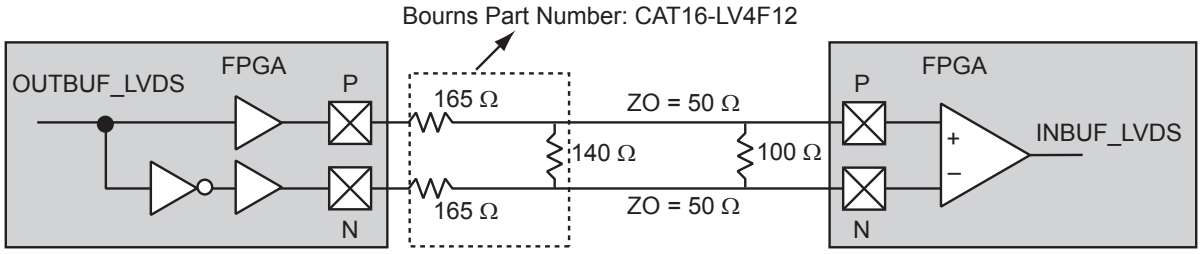


***Figure 2-128* • LVDS Circuit Diagram and Board-Level Implementation**

***Table 2-154* • LVDS Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL [4]	Output Lower Current	0.65	0.91	1.16	mA
IOH [4]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
I_{IL} [3,6]	Input High Leakage Current			10	µA
I_{IH} [3,5]	Input Low Leakage Current			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350		mV

Notes:

1. *±5%*
2. *Differential input voltage = ±350 mV*
3. *Currents are measured at 85°C junction temperature.*
4. *IOL/IOH defined by* I/O diff*/(Resistor Network)*
5. I_{IL} *is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
6. I_{IH} *is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

Table 2-155 • LVDS AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

*Note: *Measuring point = V_{trip}. See Table 2-86 on page 2-163 for a complete table of trip points.*

Timing Characteristics

Table 2-156 • LVDS
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.68	1.98	0.05	1.97	ns
–1	0.58	1.69	0.04	1.68	ns
–2	0.51	1.48	0.03	1.47	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-157 • LVDS
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.68	1.98	0.05	1.75	ns
–1	0.58	1.69	0.04	1.49	ns
–2	0.51	1.48	0.03	1.31	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations can contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The driver requires series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus, since the driver can be located anywhere on the bus. These configurations can be implemented using TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-129 on page 2-206. The input and output buffer delays are available in the LVDS section in Table 2-158 on page 2-207.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case industrial operating conditions at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

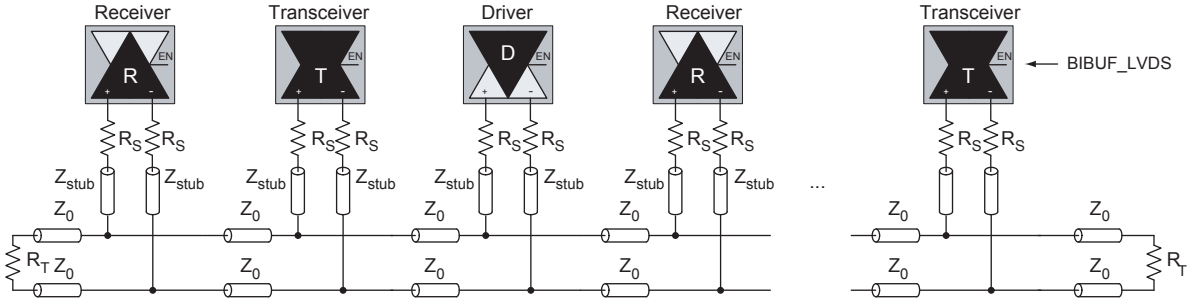


***Figure 2-129* • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-130. The building blocks of the LVPECL transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

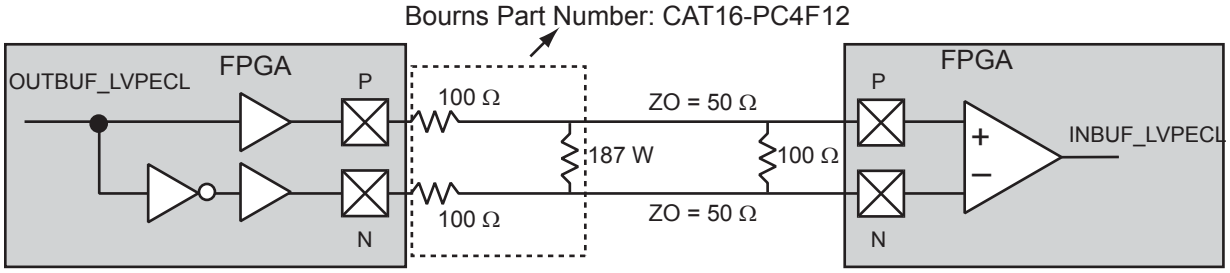


***Figure 2-130* • LVPECL Circuit Diagram and Board-Level Implementation**

***Table 2-158* • LVPECL Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.3	0	3.6	0	3.9	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

***Table 2-159* • LVPECL AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)
1.64	1.94	Cross point	–
*Note: *Measuring point = Vtrip. See Table 2-77 on page 2-150 for a complete table of trip points.*			

Timing Characteristics

***Table 2-160* • LVPECL**
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.68	1.90	0.05	1.72	ns
–1	0.58	1.61	0.04	1.47	ns
–2	0.51	1.42	0.03	1.29	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

***Table 2-161* • LVPECL**
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.68	1.90	0.05	1.48	ns
–1	0.58	1.61	0.04	1.26	ns
–2	0.51	1.42	0.03	1.11	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

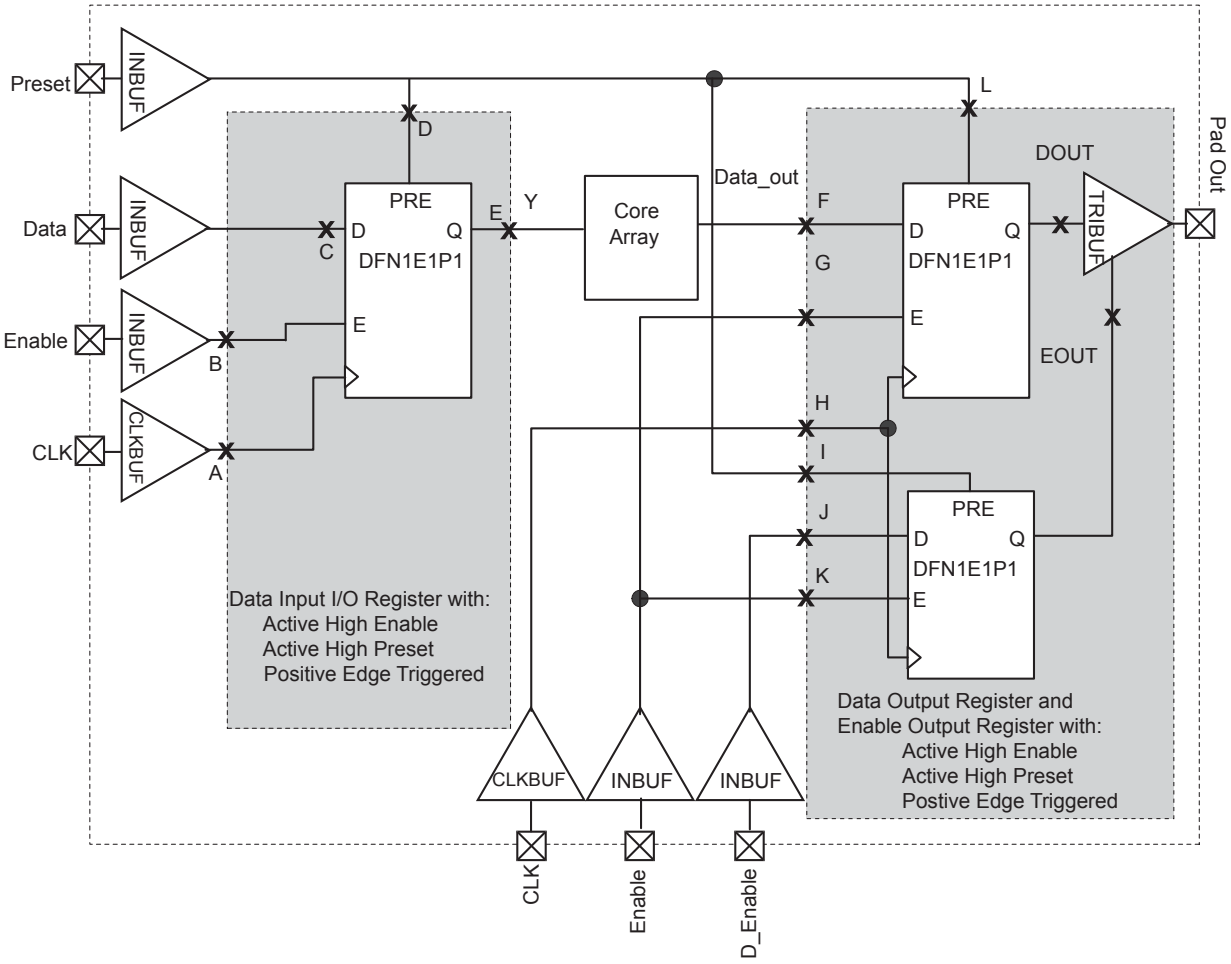


***Figure 2-131* • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

***Table 2-162* • Parameter Definitions and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L,DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

*Note: *See Figure 2-131 on page 2-208 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

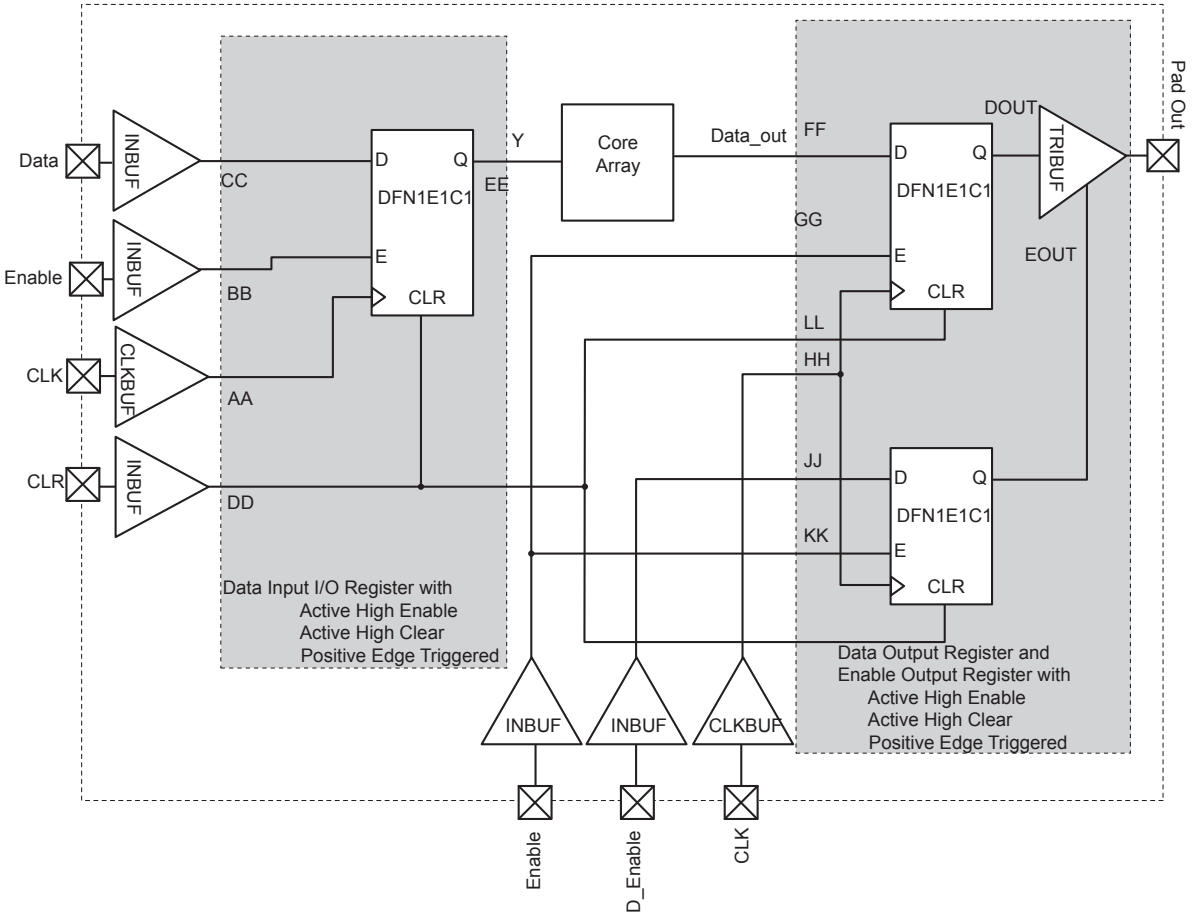


***Figure 2-132* • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

***Table 2-163* • Parameter Definitions and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

*Note: *See Figure 2-132 on page 2-210 for more information.*

Input Register

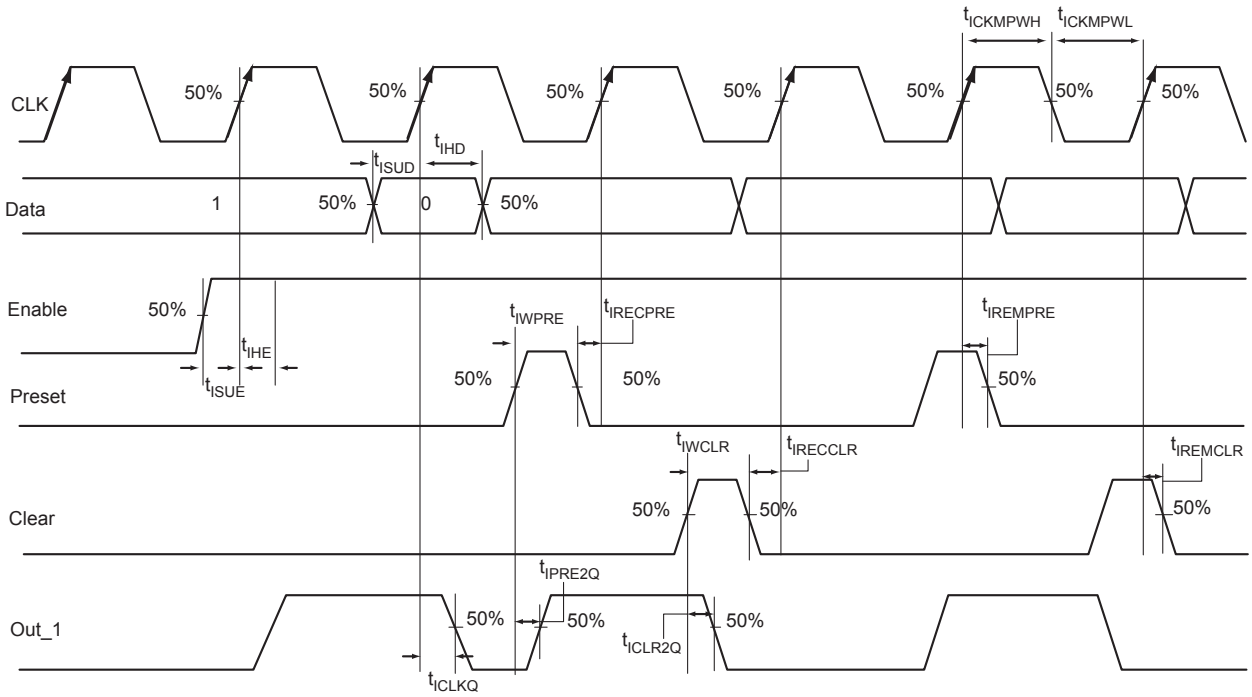


***Figure 2-133* • Input Register Timing Diagram**

Timing Characteristics

***Table 2-164* • Input Data Register Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.25	0.28	0.33	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.27	0.31	0.36	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.38	0.44	0.51	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.47	0.53	0.63	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.47	0.53	0.63	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.23	0.26	0.31	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.23	0.26	0.31	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Output Register

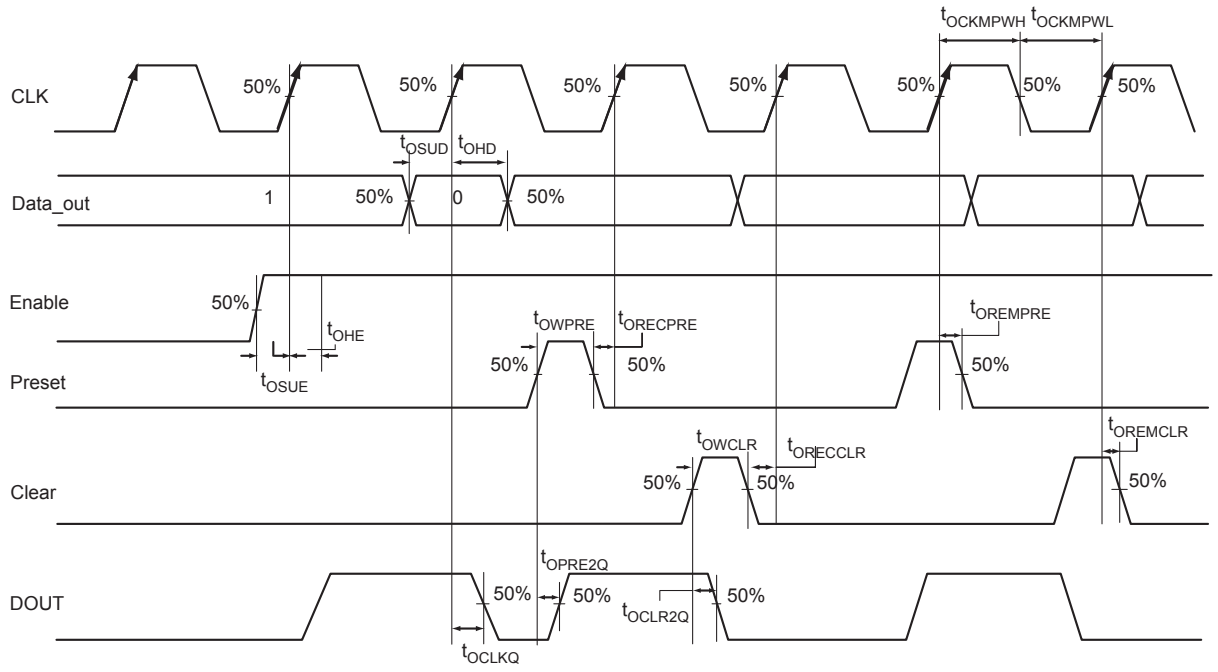


Figure 2-134 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-165 • **Output Data Register Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.61	0.69	0.81	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.37	0.43	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.45	0.51	0.60	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.83	0.94	1.11	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.83	0.94	1.11	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.26	0.31	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.26	0.31	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Output Enable Register

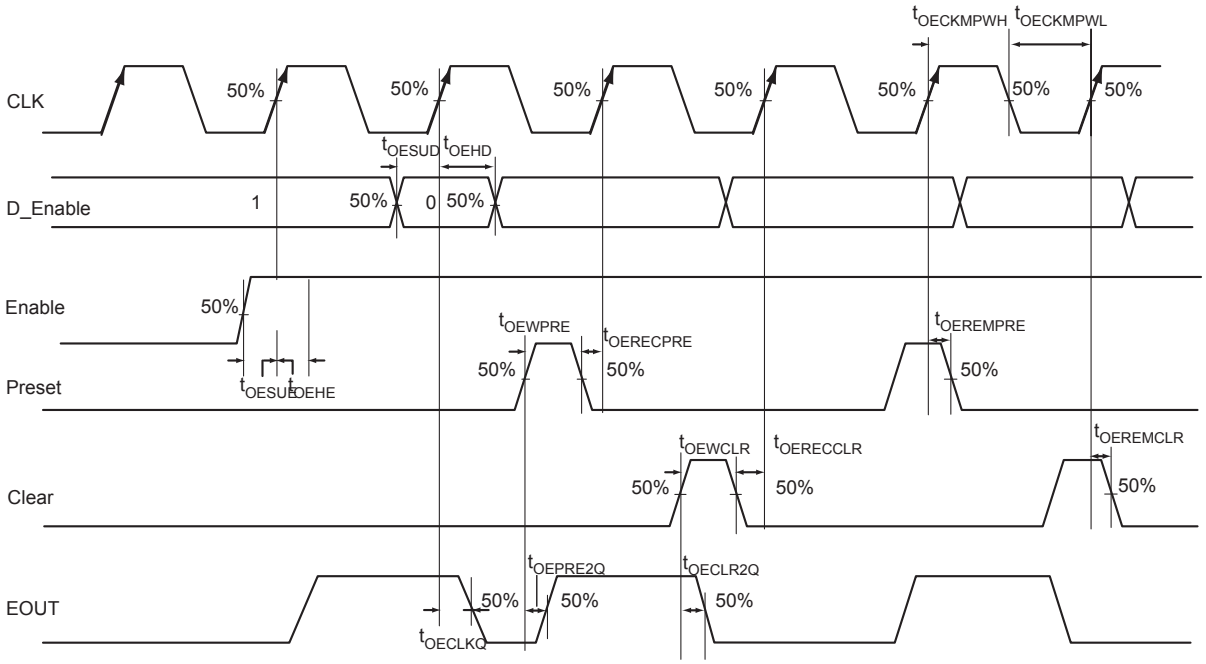


***Figure 2-135* • Output Enable Register Timing Diagram**

Timing Characteristics

***Table 2-166* • Output Enable Register Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.46	0.52	0.61	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.32	0.37	0.43	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.45	0.51	0.60	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.69	0.78	0.92	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.69	0.78	0.92	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.23	0.26	0.31	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.23	0.26	0.31	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

DDR Module Specifications

Input DDR Module

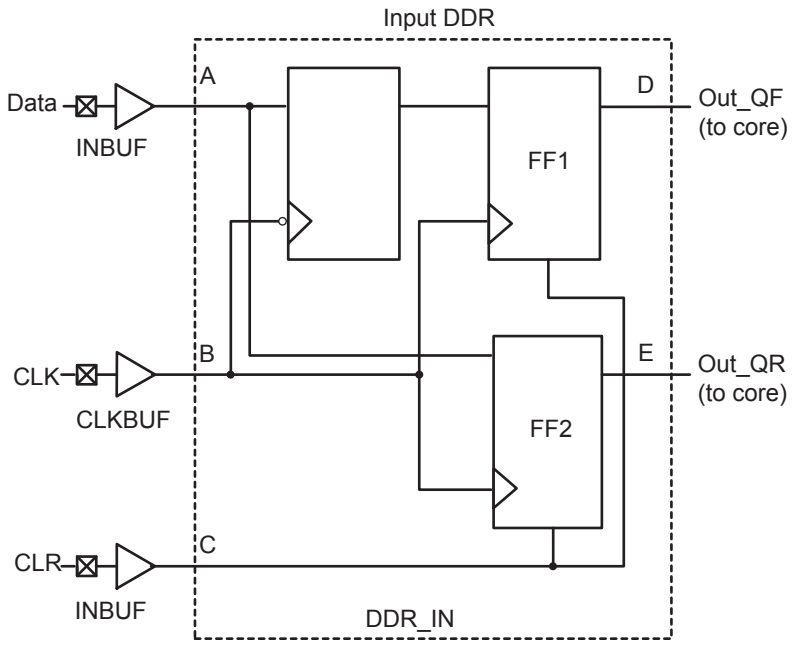


***Figure 2-136* • Input DDR Timing Model**

***Table 2-167* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR Input	A, B
t_{DDRIHD}	Data Hold Time of DDR Input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

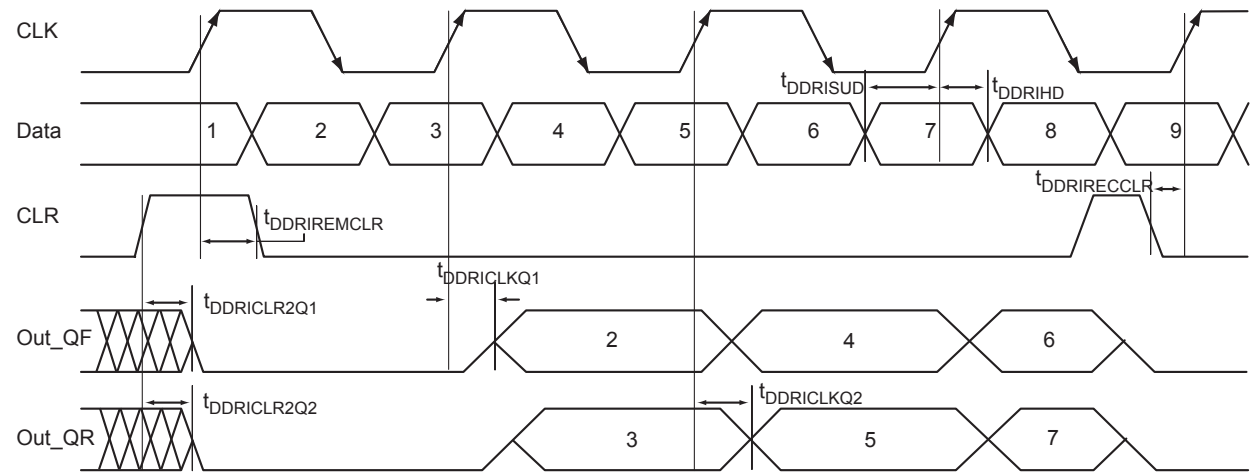


***Figure 2-137* • Input DDR Timing Diagram**

Timing Characteristics

***Table 2-168* • Input DDR Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.40	0.46	0.54	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.28	0.32	0.38	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.29	0.33	0.39	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.59	0.67	0.79	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.48	0.54	0.64	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.23	0.26	0.31	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.25	0.30	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.41	0.48	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.37	0.43	ns
FDDRIMAX	Maximum Frequency for Input DDR	1,404	1,232	1,048	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Output DDR

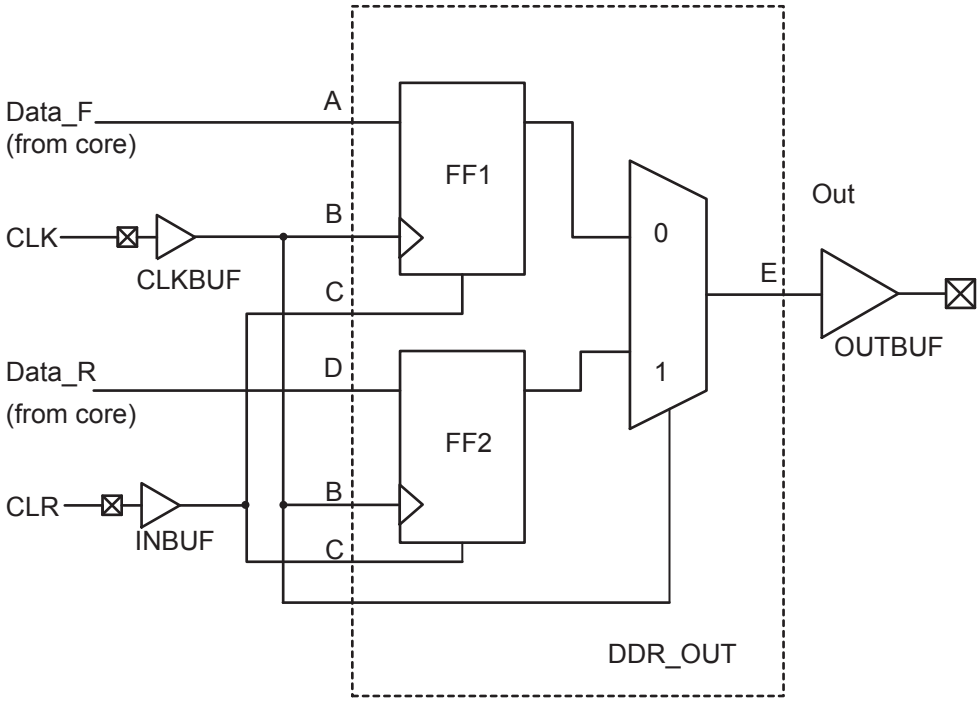


***Figure 2-138* • Output DDR Timing Model**

***Table 2-169* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

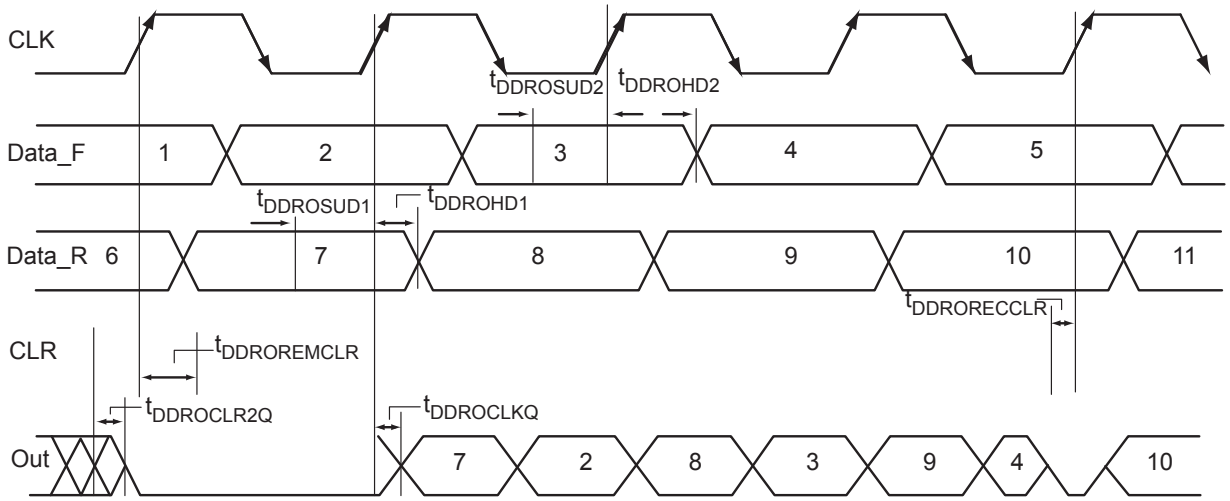


***Figure 2-139* • Output DDR Timing Diagram**

Timing Characteristics

***Table 2-170* • Output DDR Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.72	0.82	0.97	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.39	0.44	0.52	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.39	0.43	0.52	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.83	0.94	1.11	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	0.26	0.31	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	0.41	0.48	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.37	0.43	ns
FDDOMAX	Maximum Frequency for the Output DDR	1,404	1,232	1,048	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND. Note: In FG256, FG484, and FG676 packages, GNDQ and GND pins are connected within the package and are labeled as GND pins in the respective package pin assignment tables.

ADCGNDREF **Analog Reference Ground**

Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.

GNDA **Ground (analog)**

Quiet ground supply voltage to the Analog Block of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation.

GNDAQ **Ground (analog quiet)**

Quiet ground supply voltage to the analog I/O of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation. Note: In FG256, FG484, and FG676 packages, GNDAQ and GNDA pins are connected within the package and are labeled as GNDA pins in the respective package pin assignment tables. In FG256 and

GNDNVM **Flash Memory Ground**

Ground supply used by the Fusion device's flash memory block module(s).

GNDOSC **Oscillator Ground**

Ground supply for both integrated RC oscillator and crystal oscillator circuit.

VCC15A **Analog Power Supply (1.5 V)**

1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry.

VCC33A **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the 3.3 V portion of the analog circuitry.

VCC33N **Negative 3.3 V Output**

This is the –3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to ground.

VCC33PMP **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the analog charge pump. To avoid high current draw, VCC33PMP should be powered up simultaneously with or after VCC33A.

VCCNVM **Flash Memory Block Power Supply (1.5 V)**

1.5 V power supply input used by the Fusion device's flash memory block module(s). To avoid high current draw, VCC should be powered up before or simultaneously with V_{CCNVM}.

VCCOSC **Oscillator Power Supply (3.3 V)**

Power supply for both integrated RC oscillator and crystal oscillator circuit. The internal 100 MHz oscillator, powered by the VCCOSC pin, is needed for device programming, operation of the VDDN33 pump, and eNVM operation. VCCOSC is off only when VCCA is off. VCCOSC must be powered whenever the Fusion device needs to function.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a Fusion device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the Fusion device.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. B*x* is the I/O bank number. There are five (AFS600 and AFS1500) I/O banks on the Fusion devices plus a dedicated VJTAG bank.

Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VCCPLA/B **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V, where A and B refer to the PLL. The AFS600 and AFS1500 devices each have two PLLs. Actel recommends tying VCCPLX to VCC and using proper filtering circuits to decouple VCC noise from PLL.

If unused, VCCPLA/B should be tied to GND.

VCOMPLA/B **Ground for West and East PLL**

VCOMPLA is the ground of the west PLL (CCC location F) and VCOMPLB is the ground of the east PLL (CCC location C).

VJTAG **JTAG Supply Voltage**

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a Fusion device is in a JTAG chain of interconnected boards and it is desired to power down the board containing the Fusion device, this may be done provided both VJTAG and VCC to the Fusion part remain powered; otherwise, JTAG signals will not be able to transition the Fusion device, even in bypass mode.

VPUMP **Programming Supply Voltage**

Fusion devices support single-voltage ISP programming of the configuration flash and FlashROM. For programming, VPUMP should be in the 3.3 V +/-5% range. During normal device operation, VPUMP can be left floating or can be tied to any voltage between 0 V and 3.6 V.

When the VPUMP pin is tied to ground, it shuts off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

User-Defined Supply Pins

VREF **I/O Voltage Reference**

Reference voltage for I/O minibanks. Both AFS600 and AFS1500 (north bank only) support Actel Pro I/Os. These I/O banks support voltage reference standard I/O. The V_{REF} pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated as the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One V_{REF} pin can support the number of I/Os available in its minibank.

VAREF **Analog Reference Voltage**

The Fusion device can be configured to generate a 2.56 V internal reference voltage that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREF pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF is internally generated by the Fusion device, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it

takes the VAREF signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. Depending on the capacitor value selected in the Analog System Builder, a tool in Libero IDE, an automatic delay circuit will be generated using logic tiles available within the FPGA to ensure that VAREF has achieved the 2.56 V value. Actel recommends customers use 10 µF as the value of the bypass capacitor. Designers choosing to use an external VAREF need to ensure that a stable and clean VAREF source is supplied to the VAREF pin before initiating conversions by the ADC. Designers should also make sure that the ADCRESET signal is deasserted before initiating valid conversions.[2]

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are configured as inputs with pull-up resistors.

During programming, I/Os become tristated and weakly pulled up to VCCI. With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os get instantly configured to the desired user configuration.

A*xy* **Analog Input/Output**

Analog I/O pin, where *x* is the analog pad type (C = current pad, G = Gate driver pad, T = Temperature pad, V = Voltage pad) and *y* is the Analog Quad number (0 to 9). There is a minimum 1 MΩ to ground on AV, AC, and AT. This pin can be left floating when it is unused.

ATRTN*x* **Temperature Monitor Return**

AT returns are the returns for the temperature sensors. The cathode terminal of the external diodes should be connected to these pins. There is one analog return pin for every two Analog Quads. The *x* in the ATRTN*x* designator indicates the quad pairing (*x* = 0 for AQ1 and AQ2, *x* = 1 for AQ2 and AQ3, ..., *x* = 4 for AQ8 and AQ9). The signals that drive these pins are called out as ATRETURN*xy* in the software (where *x* and *y* refer to the quads that share the return signal). ATRTN is internally connected to ground. It can be left floating when it is unused. The maximum capacitance allowed across the AT pins is 500 pF.

GL **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits" section on page 2-21.

Refer to the "User I/O Naming Convention" section on page 2-156 for a description of naming of global pins.

JTAG Pins

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the Fusion part must be supplied to allow JTAG signals to transition the Fusion device.

Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND.

TCK **Test Clock**

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Actel recommends tying off TCK to GND or VJTAG through a

2. *The ADC is functional with an external reference down to 1V, however to meet the performance parameters highlighted in the datasheet refer to the VAREF specification in Table 3-2 on page 3-3.*

resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 2-171 for more information. TDITest Data Input

***Table 2-171* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance[2, 3]
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on JTAG chain.*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin can only be pulled down.*

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 2-171 and must satisfy the parallel resistance value requirement. The values in Table 2-171 correspond to the resistor recommended when a single device is used and to the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Actel recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC No Connect

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC Don't Connect

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

NCAP Negative Capacitor

Negative Capacitor is where the negative terminal of the charge pump capacitor is connected. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP.

PCAP Positive Capacitor

Positive Capacitor is where the positive terminal of the charge pump capacitor is connected. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP.

PUB **Push Button**

Push button is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

PTBASE **Pass Transistor Base**

Pass Transistor Base is the control signal of the voltage regulator. This pin should be connected to the base of the external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.

PTEM **Pass Transistor Emitter**

Pass Transistor Emitter is the feedback input of the voltage regulator.

This pin should be connected to the emitter of the external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.

XTAL1 **Crystal Oscillator Circuit Input**

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected.

XTAL2 **Crystal Oscillator Circuit Input**

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected.

Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a secure programming environment (such as the Actel in-house programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late stage product changes or personalization can be implemented easily and securely by simply sending a STAPL file with AES-encrypted data. Secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data. For more information, refer to the *Fusion Security* application note.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-197) block cipher is the National Institute of Standards and Technology (NIST) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4×10^{38} possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (securely) in Fusion devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain secure.

AES decryption can also be used on the 1,024-bit FlashROM to allow for secure remote updates of the FlashROM contents. This allows for easy, secure support for subscription model products. See the application note *Fusion Security* for more details.

AES for Flash Memory

AES decryption can also be used on the flash memory blocks. This allows for the secure update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Actel).

The user can generate STP programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in-system. During programming, VCCOSC is needed in order to power the internal 100 MHz oscillator. This oscillator is used as a source for the 20 MHz oscillator that is used to drive the charge pump for programming.

ISP

Fusion devices support IEEE 1532 ISP via JTAG and require a single VPUMP voltage of 3.3 V during programming. In addition, programming via a microcontroller in a target system can be achieved. Refer to the standard or the "In-System Programming (ISP) of Actel's Low Power Flash Devices Using FlashPro4/3/3X" chapter of the *Fusion FPGA Fabric User's Guide* for more details.

JTAG IEEE 1532

Programming with IEEE 1532

Fusion devices support the JTAG-based IEEE1532 standard for ISP. As part of this support, when a Fusion device is in an unprogrammed state, all user I/O pins are disabled. This is achieved by keeping the global IO_EN signal deactivated, which also has the effect of disabling the input buffers. Consequently, the SAMPLE instruction will have no effect while the Fusion device is in this unprogrammed state—different behavior from that of the ProASIC PLUS® device family. This is done

because SAMPLE is defined in the IEEE1532 specification as a noninvasive instruction. If the input buffers were to be enabled by SAMPLE temporarily turning on the I/Os, then it would not truly be a noninvasive instruction. Refer to the standard or the "In-System Programming (ISP) of Actel's Low Power Flash Devices Using FlashPro4/3/3X" chapter of the *Fusion FPGA Fabric User's Guide* for more details.

Boundary Scan

Fusion devices are compatible with IEEE Standard 1149.1, which defines a hardware architecture and the set of mechanisms for boundary scan testing. The basic Fusion boundary scan logic circuit is composed of the test access port (TAP) controller, test data registers, and instruction register (Figure 2-140 on page 2-226). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instruction (Table 2-173 on page 2-226).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, TDO (test data input and output), TMS (test mode selector), and TRST (test reset input). TMS, TDI, and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary scan test usage. Refer to the "JTAG Pins" section on page 2-221 for pull-up/-down recommendations for TDO and TCK pins. The TAP controller is a 4-bit state machine (16 states) that operates as shown in Figure 2-140 on page 2-226. The 1s and 0s represent the values that must be present on TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

***Table 2-172* • TRST and TCK Pull-Down Recommendations**

VJTAG	Tie-Off Resistance*
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

*Note: *Equivalent parallel resistance if more than one device is on JTAG chain.*

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain High for five TCK cycles. The TRST pin can also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

Fusion devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (LSB, ID number, part number, and version). The boundary scan register observes and controls the state of each I/O pin. Each I/O cell has three boundary scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin.

The serial pins are used to serially connect all the boundary scan register cells in a device into a boundary scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

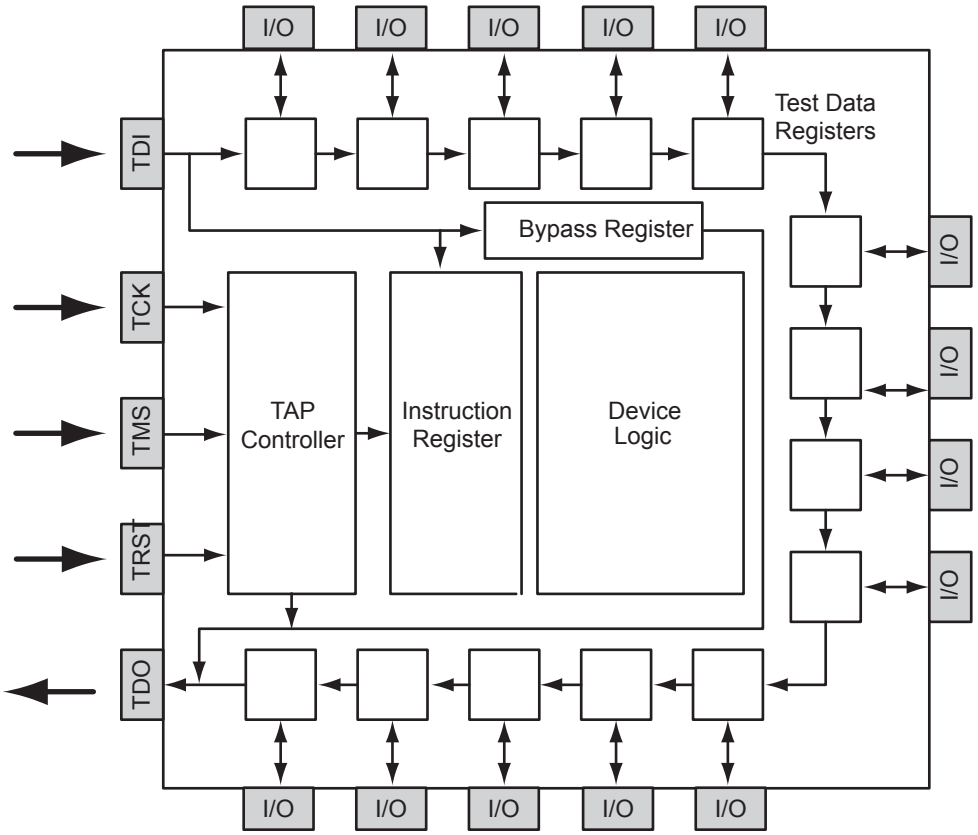


***Figure 2-140* • Boundary Scan Chain in Fusion**

***Table 2-173* • Boundary Scan Opcodes**

	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF

IEEE 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/Os" section on page 2-130 for more details.

Timing Characteristics

***Table 2-174* • JTAG 1532**
Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.50	0.58	0.68	ns
t_{DIHD}	Test Data Input Hold Time	1.00	1.15	1.35	ns
t_{TMSSU}	Test Mode Select Setup Time	0.50	0.58	0.68	ns
t_{TMDHD}	Test Mode Select Hold Time	1.00	1.15	1.35	ns
t_{TCK2Q}	Clock to Q (data out)	6.00	5.75	6.77	ns
t_{RSTB2Q}	Reset to Q (data out)	20.00	23.00	27.06	ns
FTCKMAX	TCK Maximum Frequency	25.00	23.00	20.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.20	0.23	0.27	ns
$t_{TRSTMPW}$	ResetB minimum pulse	TBD	TBD	TBD	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

3 – DC and Power Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in Table 3-2 on page 3-3.

Table 3-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limit	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage [1]	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
VCC33A	+3.3 V power supply	–0.3 to 3.75 [2]	V
VCC33PMP	+3.3 V power supply	–0.3 to 3.75 [2]	V
VAREF	Voltage reference for ADC	–0.3 to 3.75	V
VCC15A	Digital power supply for the analog system	–0.3 to 1.65	V
VCCNVM	Embedded flash power supply	–0.3 to 1.65	V
VCCOSC	Oscillator power supply	–0.3 to 3.75	V

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-5.*
2. *Analog data not valid beyond 3.65 V.*
3. *The high current mode has a maximum power limit of 15 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
4. *For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.*
5. *Negative input is not supported between –40°C and –55°C.*
6. *Positive input is not supported between –40°C and –55°C.*

Table 3-1 • **Absolute Maximum Ratings (continued)**

Symbol	Parameter	Limit	Units
AV	Unpowered, ADC reset asserted or unconfigured	–11.0 to 12.0	V
	Analog input (+16 V to +2 V prescaler range)	–0.4 to 12.0	V
	Analog input (+1 V to +0.125 V prescaler range)	–0.4 to 3.75	V
	Analog input (–16 V to –2 V prescaler range)[5]	–11.0 to 0.4	V
	Analog input (–1 V to –0.125 V prescaler range)[5]	–3.75 to 0.4	V
	Analog input (direct input to ADC)	–0.4 to 3.75	V
	Analog input (positive current monitor)[6]	–0.4 to 12.0	V
	Analog input (negative current monitor)[5]	–11.0 to 0.4	V
	Digital input	–0.4 to 12.0	V
AC	Unpowered, ADC reset asserted or unconfigured	–11.0 to 12.0	V
	Analog input (+16 V to +2 V prescaler range)	–0.4 to 12.0	V
	Analog input (+1 V to +0.125 V prescaler range)	–0.4 to 3.75	V
	Analog input (–16 V to –2 V prescaler range)[5]	–11.0 to 0.4	V
	Analog input (–1 V to –0.125 V prescaler range)[5]	–3.75 to 0.4	V
	Analog input (direct input to ADC)	–0.4 to 3.75	V
	Analog input (positive current monitor)[6]	–0.4 to 12.0	V
	Analog input (negative current monitor)[5]	–11.0 to 0.4	V
	Digital input	–0.4 to 12.0	V
AG	Unpowered, ADC reset asserted or unconfigured	–11.0 to 12.0	V
	Low Current Mode (1 µA, 3 µA, 10 µA, 30 µA)	–0.4 to 12.0	V
	Low Current Mode (–1 µA, –3 µA, –10 µA, –30 µA)	–11.0 to 0.4	V
	High Current Mode [3]	–11.0 to 12.0	V
AT	Unpowered, ADC reset asserted or unconfigured	–0.4 to 15.0	V
	Analog input (+16 V, 4 V prescaler range)	–0.4 to 15.0	V
	Analog input (direct input to ADC)	–0.4 to 3.75	V
	Digital input	–0.4 to 1650	V
T_{STG} [4]	Storage temperature	–65 to 150	°C
T_J [4]	Junction temperature	125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-5.*
2. *Analog data not valid beyond 3.65 V.*
3. *The high current mode has a maximum power limit of 15 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
4. *For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.*
5. *Negative input is not supported between –40°C and –55°C.*
6. *Positive input is not supported between –40°C and –55°C.*

Table 3-2 • **Recommended Operating Conditions[2]**

Symbol	Parameter		Ext. Temperature	Units
T_J	Junction temperature		–55 to +100	°C
VCC	1.5 V DC core supply voltage		1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	V
VPUMP	Programming voltage	Programming mode	3.15 to 3.45	V
		Operation[3]	0 to 3.6	V
VCCPLL	Analog power supply (PLL)		1.425 to 1.575	V
VCCI	1.5 V DC supply voltage		1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	V
VCC33A	+3.3 V power supply		2.97 to 3.63	V
VCC33PMP	+3.3 V power supply		2.97 to 3.63	V
VAREF	Voltage reference for ADC		2.527 to 2.593	V
VCC15A [6]	Digital power supply for the analog system		1.425 to 1.575	V
VCCNVM	Embedded flash power supply		1.425 to 1.575	V
VCCOSC	Oscillator power supply		2.97 to 3.63	V
AV	Unpowered, ADC reset asserted or unconfigured		–10.5 to 11.6	V
	Analog input (+16 V to +2 V prescaler range)		–0.3 to 11.6	V
	Analog input (+1 V to + 0.125 V prescaler range)		–0.3 to 3.6	V
	Analog input (–16 V to –2 V prescaler range)[7]		–10.5 to 0.3	V
	Analog input (–1 V to –0.125 V prescaler range)[7]		–3.6 to 0.3	V
	Analog input (direct input to ADC)		–0.3 to 3.6	V
	Analog input (positive current monitor)[8]		–0.3 to 11.6	V
	Analog input (negative current monitor)[7]		–10.5 to 0.3	V
	Digital input		–0.3 to 11.6	V

Notes:

1. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-82 on page 2-155.*
2. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
3. *VPUMP can be left floating during normal operation (not programming mode).*
4. *The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.*
5. *The AG pad should also conform to the limits as specified in Table 2-44 on page 2-106.*
6. *Violating the VCC15A recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.*
7. *Negative input is not supported between –40°C and –55°C.*
8. *Positive input is not supported between –40°C and –55°C.*

Table 3-2 • **Recommended Operating Conditions[2] (continued)**

Symbol	Parameter	Ext. Temperature	Units
AC	Unpowered, ADC reset asserted or unconfigured	–10.5 to 11.6	V
	Analog input (+16 V to +2 V prescaler range)	–0.3 to 11.6	V
	Analog input (+1 V to +0.125 V prescaler range)	–0.3 to 3.6	V
	Analog input (–16 V to –2 V prescaler range)	–10.5 to 0.3	V
	Analog input (–1 V to –0.125 V prescaler range)	–3.6 to 0.3	V
	Analog input (direct input to ADC)	–0.3 to 3.6	V
	Analog input (positive current monitor)[8]	–0.3 to 11.6	V
	Analog input (negative current monitor)[7]	–10.5 to 0.3	V
	Digital input	–0.3 to 11.6	V
AG [4,5]	Unpowered, ADC reset asserted or unconfigured	–10.5 to 11.6	V
	Low Current Mode (1 µA, 3 µA, 10 µA, 30 µA)	–0.3 to 11.6	V
	Low Current Mode (–1 µA, –3 µA, –10 µA, –30 µA)	–10.5 to 0.3	V
	High Current Mode [5]	–10.5 to 11.6	V
AT [4]	Unpowered, ADC reset asserted or unconfigured	–0.3 to 14.5	V
	Analog input (+16 V, +4 V prescaler range)	–0.3 to 14.5	V
	Analog input (direct input to ADC)	–0.3 to 3.6	V
	Digital input	–0.3 to 14.5	V

Notes:

1. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-82 on page 2-155.*
2. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
3. *VPUMP can be left floating during normal operation (not programming mode).*
4. *The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.*
5. *The AG pad should also conform to the limits as specified in Table 2-44 on page 2-106.*
6. *Violating the VCC15A recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.*
7. *Negative input is not supported between –40°C and –55°C.*
8. *Positive input is not supported between –40°C and –55°C.*

Table 3-3 • Input Resistance of Analog Pads

Pads	Pad Configuration	Prescaler Range	Input Resistance to Ground
AV	Analog Input (direct input to ADC)	+16 V to +2 V	1 MΩ (typical)
		+1 V to +0.125 V	> 10 MΩ
	Analog Input (positive prescaler)	+16 V to +2 V	1 MΩ (typical)
		+1 V to +0.125 V	> 10 MΩ
	Analog Input (negative prescaler)	–16 V to –2 V	1 MΩ (typical)
		–1 V to –0.125 V	> 10 MΩ
	Digital input	+16 V to +2 V	1 MΩ (typical)
	Current monitor	+16 V to +2 V	1 MΩ (typical)
		–16 V to –2 V	1 MΩ (typical)
AT	Analog Input (direct input to ADC)	+16 V, +4 V	1 MΩ (typical)
	Analog Input (positive prescaler)	+16 V, +4 V	1 MΩ (typical)
	Digital input	+16 V, +4 V	1 MΩ (typical)
	Temperature monitor	+16 V, +4 V	> 10 MΩ

Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os)[1]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3.0 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at a junction temperature of 85°C.*
2. *The duration is allowed at one cycle out of six clock cycle. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

Table 3-5 • FPGA Programming, Storage, and Operating Limits

Product Grade	Storage Temperature	Element	Grade Programming Cycles	Retention
Extended Temperature (K)	Min. T_J = –55°C	FPGA/FlashROM	500	20 years
	Min. T_J = 100°C	Embedded flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset

Sophisticated power-up management circuitry is designed into every Fusion device. These circuits ensure easy transition from the powered off state to the powered up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 3-1 on page 3-7.

There are five regions to consider during power-up.

Fusion I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 3-1).
2. VCCI > VCC – 0.75 V (typical).
3. Chip is in the operating mode.

VCCI **Trip Point:**

Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC **Trip Point:**

Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

PLL Behavior at Brownout Condition

Actel recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 3-1 on page 3-7 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost.

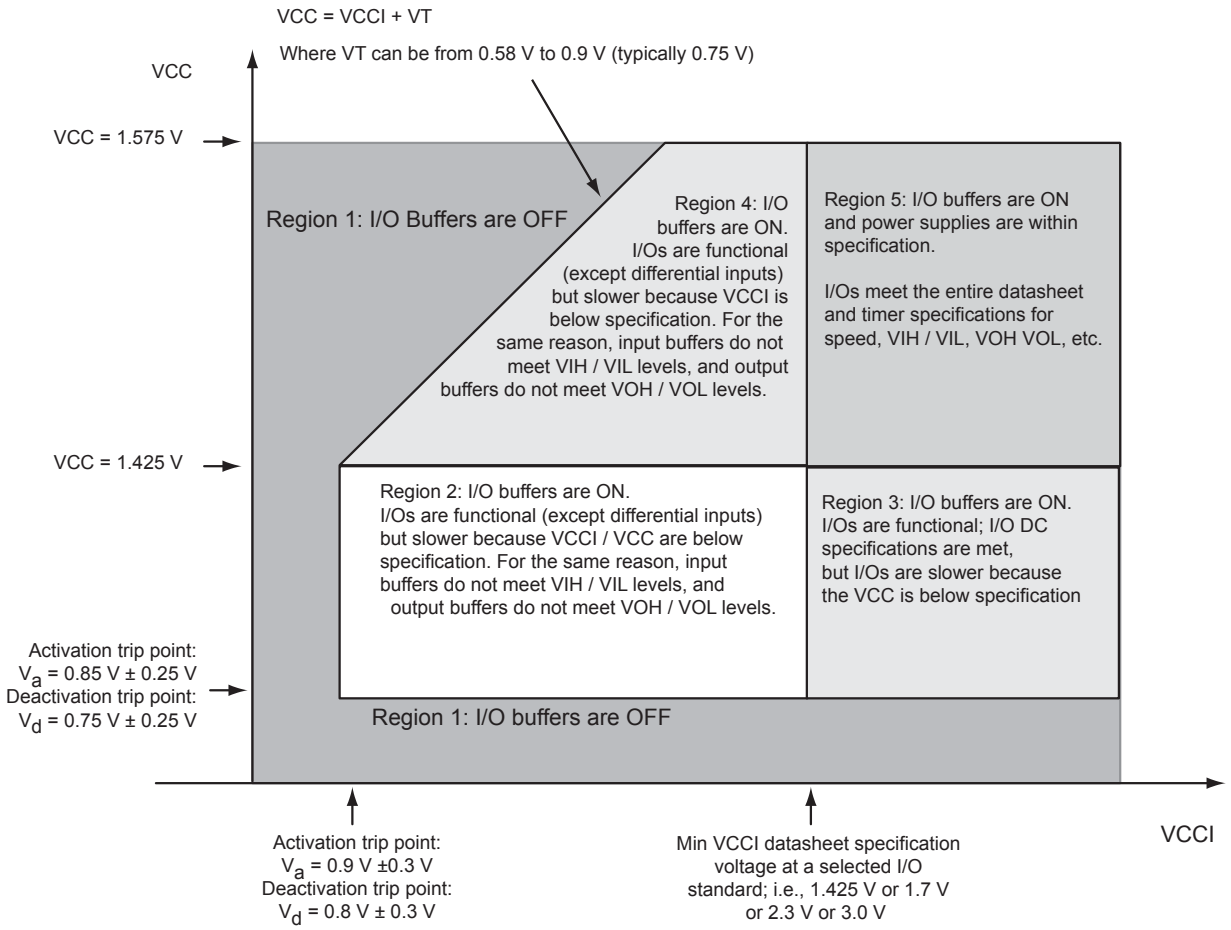


Figure 3-1 • **I/O State as a Function of VCCI and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 3-6 • **Package Thermal Resistance**

Product	Die Size (mm)	θ_{JA}			θ_{JC}	θ_{JB}	Units
		Still Air	1.0 m/s	2.5 m/s			
AFS600-FG256	X = 5.10; Y = 7.3	28.9	25.2	23.5	6.8	19.9	°C/W
AFS1500-FG256	X = 7.62; Y = 9.98	23.3	19.6	18.0	4.3	14.2	°C/W
AFS600-FG484	X = 5.10; Y = 7.3	21.8	18.2	16.7	7.7	16.8	°C/W
AFS1500-FG484	X = 7.62; Y = 9.98	21.6	16.8	15.2	5.6	14.9	°C/W

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

θ_{JA} = 19.00°C/W (taken from Table 3-6 on page 3-8).

T_A = 75.00°C

$$\text{Maximum Power Allowed} = \frac{100.00°C - 75.00°C}{19.00°C/W} = 1.3\ W$$

EQ 5

The power consumption of a device can be calculated using the Actel power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

T_J = 100.00°C

T_A = 70.00°C

From the datasheet:

θ_{JA} = 17.00°C/W

θ_{JC} = 8.28°C/W

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{17.00\ W} = 1.76\ W$$

EQ 6

The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{ja(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

θ_{JA} = 0.37°C/W

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 13.33°C/W - 8.28°C/W - 0.37°C/W = 5.01°C/W$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 3-7 • **Temperature and Voltage Derating Factors for Timing Delays (Normalized to T_J = 100°C, Worst-Case VCC = 1.425 V)**

Array Voltage VCC (V)	Junction Temperature (°C)						
	–55°C	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**100°C**
1.425	0.83	0.85	0.89	0.92	0.97	0.98	1.00
1.500	0.78	0.80	0.85	0.87	0.91	0.93	0.95
1.575	0.76	0.77	0.82	0.84	0.88	0.90	0.91

Calculating Power Dissipation

Quiescent Supply Current

Table 3-8 • **AFS1500 Quiescent Supply Current Characteristics**

Parameter	Description	Conditions	Temp.	Min.	Typ.	Max.	Unit
I_{CC}[1]	1.5 V quiescent current	Operational standby[4], VCC = 1.575 V	T_J = 25°C		20	40	mA
			T_J = 85°C		32	65	mA
			T_J = 100°C		59	120	mA
		Standby mode[5] or Sleep mode[6], VCC = 0 V			0	0	µA
I_{CC33}[2]	3.3 V analog supplies current	Operational standby[4], VCC33 = 3.63 V	T_J = 25°C		9.8	13	mA
			T_J = 85°C		10.7	14	mA
			T_J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T_J = 25°C		0.31	2	mA
			T_J = 85°C		0.35	2	mA
			T_J = 100°C		0.45	2	mA
		Standby mode[5], VCC33 = 3.63 V	T_J = 25°C		2.9	3.6	mA
			T_J = 85°C		2.9	4	mA
			T_J = 100°C		3.3	6	mA
		Sleep mode[6], VCC33 = 3.63 V	T_J = 25°C		17	19	µA
			T_J = 85°C		18	20	µA
			T_J = 100°C		24	25	µA
I_{CCI}[3]	I/O quiescent current	Operational standby[4], Standby mode, and Sleep Mode[6], VCCIx = 3.63 V	T_J = 25°C		417	649	µA
			T_J = 85°C		417	649	µA
			T_J = 100°C		417	649	µA

Notes:

1. *I_{CC} is the 1.5 V power supplies, I_{CC} and I_{CC15A}.*
2. *I_{CC33A} includes I_{CC33A}, $I_{CC33PMP}$, and I_{CCOSC}.*
3. *I_{CCI} includes all I_{CCI0}, I_{CCI1}, I_{CCI2}, and I_{CCI4}.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = V_{PP} = 0 V. Sleep mode is not supported between –40°C and –55°C*

Table 3-8 • **AFS1500 Quiescent Supply Current Characteristics (continued)**

Parameter	Description	Conditions	Temp.	Min.	Typ.	Max.	Unit
I_{JTAG}	JTAG I/O quiescent current	Operational standby[4], VJTAG = 3.63 V	T_J = 25°C		80	100	µA
			T_J = 85°C		80	100	µA
			T_J = 100°C		80	100	µA
		Standby mode[5] or Sleep mode[6], VJTAG = 0 V			0	0	µA
I_{PP}	Programming supply current	Non-programming mode, VPP = 3.63 V	T_J = 25°C		39	80	µA
			T_J = 85°C		40	80	µA
			T_J = 100°C		40	80	µA
		Standby mode[5] or Sleep mode[6], VPP = 0 V			0	0	µA
I_{CCNVM}	Embedded NVM current	Reset asserted, VCCNVM = 1.575 V	T_J = 25°C		50	150	µA
			T_J =85°C		50	150	µA
			T_J = 100°C		50	150	µA
I_{CCPLL}	1.5 V PLL quiescent current	Operational standby, VCCPLL = 1.575 V	T_J = 25°C		130	200	µA
			T_J = 85°C		130	200	µA
			T_J = 100°C		130	200	µA

Notes:

1. *I_{CC} is the 1.5 V power supplies, I_{CC} and I_{CC15A}.*
2. *I_{CC33A} includes I_{CC33A}, $I_{CC33PMP}$, and I_{CCOSC}.*
3. *I_{CCI} includes all I_{CCI0}, I_{CCI1}, I_{CCI2}, and I_{CCI4}.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = V_{PP} = 0 V. Sleep mode is not supported between –40°C and –55°C*

Table 3-9 • **AFS600 Quiescent Supply Current Characteristics**

Parameter	Description	Conditions	Temp.	Min	Typ	Max	Unit
I_{CC}[1]	1.5 V quiescent current	Operational standby[4], VCC = 1.575 V	T_J = 25°C		13	25	mA
			T_J = 85°C		20	45	mA
			T_J=100°C		25	75	mA
		Standby mode[5] or Sleep mode[6], VCC = 0 V			0	0	µA
I_{CC33}[2]	3.3 V analog supplies current	Operational standby[4], VCC33 = 3.63 V	T_J = 25°C		9.8	13	mA
			T_J = 85°C		10.7	14	mA
			T_J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T_J = 25°C		0.31	2	mA
			T_J = 85°C		0.35	2	mA
			T_J = 100°C		0.45	2	mA
		Standby mode[5], VCC33 = 3.63 V	T_J = 25°C		2.8	3.6	mA
			T_J = 85°C		2.9	4	mA
			T_J = 100°C		3.5	6	mA
		Sleep mode[6], VCC33 = 3.63 V	T_J = 25°C		17	19	µA
			T_J = 85°C		18	20	µA
			T_J = 100°C		24	25	µA
I_{CCI}[3]	I/O quiescent current	Operational standby,[4] VCCIx = 3.63 V	T_J = 25°C		417	648	µA
			T_J = 85°C		417	648	µA
			T_J = 100°C		417	649	µA
I_{JTAG}	JTAG I/O quiescent current	Operational standby,[4] VJTAG = 3.63 V	T_J = 25°C		80	100	µA
			T_J = 85°C		80	100	µA
			T_J = 100°C		80	100	µA
		Standby mode[5] or Sleep mode[6], VJTAG = 0 V			0	0	µA

Notes:

1. *I_{CC} is the 1.5 V power supplies, I_{CC} and I_{CC15A}.*
2. *I_{CC33A} includes I_{CC33A}, $I_{CC33PMP}$, and I_{CCOSC}.*
3. *I_{CCI} includes all I_{CCI0}, I_{CCI1}, I_{CCI2}, and I_{CCI4}.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPP = 0 V. Sleep mode is not supported between –40°C and –55°C.*

Table 3-9 • **AFS600 Quiescent Supply Current Characteristics (continued)**

Parameter	Description	Conditions	Temp.	Min	Typ	Max	Unit
I_{PP}	Programming supply current	Non-programming mode, VPP = 3.63 V	T_J = 25°C		36	80	µA
			T_J = 85°C		36	80	µA
			T_J = 100°C		36	80	µA
		Standby mode[5] or Sleep mode[6], V_{PP} = 0 V			0	0	µA
I_{CCNVM}	Embedded NVM current	Reset asserted, VCCNVM = 1.575 V	T_J = 25°C		22	80	µA
			T_J = 85°C		24	80	µA
			T_J = 100°C		25	80	µA
I_{CCPLL}	1.5 V PLL quiescent current	Operational standby, VCCPLL = 1.575 V	T_J = 25°C		130	200	µA
			T_J = 85°C		130	200	µA
			T_J = 100°C		130	200	µA

Notes:

1. *I_{CC} is the 1.5 V power supplies, I_{CC} and I_{CC15A}.*
2. *I_{CC33A} includes I_{CC33A}, $I_{CC33PMP}$, and I_{CCOSC}.*
3. *I_{CCI} includes all I_{CCI0}, I_{CCI1}, I_{CCI2}, and I_{CCI4}.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPP = 0 V. Sleep mode is not supported between –40°C and –55°C.*

Power per I/O Pin

***Table 3-10* • Summary of I/O Input Buffer Power (per pin)—Default I/O Software Settings**

	VMV (V)	Static Power PDC7 (mW)1	Dynamic Power PAC9 (µW/MHz)2
Applicable to Pro I/O Banks			
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS – Schmitt trigger	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	0.98
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	36.11
2.5 V GTL	2.5	2.13	24.87
3.3 V GTL+	3.3	2.81	31.02
2.5 V GTL+	2.5	2.57	28.30
HSTL (I)	1.5	0.17	2.50
HSTL (II)	1.5	0.17	2.50
SSTL2 (I)	2.5	1.38	17.05
SSTL2 (II)	2.5	1.38	17.05
SSTL3 (I)	3.3	3.21	40.09
SSTL3 (II)	3.3	3.21	40.09
Differential			
LVDS	2.5	2.26	1.05
LVPECL	3.3	5.71	118.08

Notes:

1. *PDC7 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VCC and VMV.*

***Table 3-10* • Summary of I/O Input Buffer Power (per pin)—Default I/O Software Settings (continued)**

	VMV (V)	Static Power PDC7 (mW)1	Dynamic Power PAC9 (µW/MHz)2
Applicable to Advanced I/O Banks			
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	16.22
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.66
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64
Differential			
LVDS	2.5	2.26	46.90
LVPECL	3.3	5.72	118.10

Notes:

1. *PDC7 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VCC and VMV.*

Table 3-11 • **Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings[1]**

	CLOAD (pF)	VCCI (V)	Static Power PDC8 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Applicable to Pro I/O Banks				
Single-Ended				
3.3 V LVTTL/LVCMOS	35	3.3	–	474.70
2.5 V LVCMOS	35	2.5	–	270.73
1.8 V LVCMOS	35	1.8	–	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.55
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.18
SSTL2 (I)	30	2.5	16.69	105.65
SSTL2 (II)	30	2.5	25.91	116.48
SSTL3 (I)	30	3.3	26.02	114.67
SSTL3 (II)	30	3.3	42.21	131.69
Differential				
LVDS	–	2.5	7.70	90.17
LVPECL	–	3.3	19.42	168.70
Applicable to Advanced I/O Banks				
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	466.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.55
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	89.82
LVPECL	–	3.3	19.54	167.55

Notes:

1. *Dynamic power consumption is given for standard load and software-default drive strength and output slew.*
2. *PDC8 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCC and VCCI.*

Dynamic Power Consumption of Various Internal Resources

***Table 3-12* • Different Components Contributing to the Dynamic Power Consumption in Fusion Devices**

Parameter	Definition	Power Supply		Device-Specific Dynamic Contributions		Units
		Name	Setting	AFS1500	AFS600	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	14.5	12.8	µW/MHz
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	2.5	1.9	µW/MHz
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V	0.81		µW/MHz
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.11		µW/MHz
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.07		µW/MHz
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.29		µW/MHz
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V	0.29		µW/MHz
PAC8	Average contribution of a routing net	VCC	1.5 V	0.70		µW/MHz
PAC9	Contribution of an I/O input pin (standard dependent)	VCCI	See Table 3-10 on page 3-15			
PAC10	Contribution of an I/O output pin (standard dependent)	VCCI	See Table 3-11 on page 3-17			
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V	25		µW/MHz
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V	30		µW/MHz
PAC13	Dynamic Contribution for PLL	VCC	1.5 V	2.6		µW/MHz
PAC15	Contribution of NVM block during a read operation (F < 33MHz)	VCC	1.5 V	358		µW/MHz
PAC16	1st contribution of NVM block during a read operation (F > 33 MHz)	VCC	1.5 V	12.88		mW
PAC17	2nd contribution of NVM block during a read operation (F > 33 MHz)	VCC	1.5 V	4.8		µW/MHz
PAC18	Crystal Oscillator contribution	VCC33A	3.3 V	0.63		mW
PAC19	RC Oscillator contribution	VCC33A	3.3 V	3.3		mW
PAC20	Analog Block dynamic power contribution of ADC	VCC	1.5 V	3		mW

Static Power Consumption of Various Internal Resources

***Table 3-13* • Different Components Contributing to the Static Power Consumption in Fusion Devices**

Parameter	Definition	Power Supply		Device-Specific Static Contributions		Units
		Name	Setting	AFS1500	AFS600	
PDC1	Core static power contribution in operating mode	VCC	1.5 V	18	7.5	mW
PDC2	Device static power contribution in sleep mode*	VCC33A	3.3 V	0.66		mW
PDC3	Device static power contribution in standby mode	VCC33A	3.3 V	0.03		mW
PDC4	NVM static power contribution	VCC	1.5 V	1.19		mW
PDC5	Analog Block static power contribution of ADC	VCC33A	3.3 V	8.25		mW
PDC6	Analog Block static power contribution per Quad	VCC33A	3.3 V	3.3		mW
PDC7	Static contribution per input pin – standard dependent contribution	VCCI	See Table 3-10 on page 3-15			
PDC8	Static contribution per output pin – standard dependent contribution	VCCI	See Table 3-11 on page 3-17			
PDC9	Static contribution for PLL	VCC	1.5 V	2.55		mW

*Note: *Sleep mode is not supported between –40°C and –55°C.*

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of NVM blocks used in the design
- The number of Analog Quads used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 3-14 on page 3-23.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 3-15 on page 3-23.
- Read rate and write rate to the RAM—guidelines are provided for typical applications in Table 3-15 on page 3-23.
- Read rate to the NVM blocks

The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

Operating Mode, Standby Mode, and Sleep Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

Operating Mode

$P_{STAT} = P_{DC1} + (N_{NVM\text{-}BLOCKS} * P_{DC4}) + P_{DC5} + (N_{QUADS} * P_{DC6}) + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8}) + (N_{PLLS} * P_{DC9})$

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks available in the device.

N_{QUADS} is the number of Analog Quads used in the design.

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = P_{DC2}$

Sleep Mode

$P_{STAT} = P_{DC3}$

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB}$

Standby Mode

$P_{DYN} = P_{XTL\text{-}OSC}$

Sleep Mode

$P_{DYN} = 0$ W

Global Clock Dynamic Contribution—P_{CLOCK}

Operating Mode

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * PAC3 + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in Table 3-14 on page 3-23.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in Table 3-14 on page 3-23.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Sleep Mode

$P_{CLOCK} = 0$ W

Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

Operating Mode

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + (\alpha_1 / 2) * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-14 on page 3-23.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$P_{S\text{-}CELL}$ = 0 W

Combinatorial Cells Dynamic Contribution—$P_{C\text{-}CELL}$

Operating Mode

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-14 on page 3-23.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$P_{C\text{-}CELL}$ = 0 W

Routing Net Dynamic Contribution—P_{NET}

Operating Mode

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-14 on page 3-23.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

P_{NET} = 0 W

I/O Input Buffer Dynamic Contribution—P_{INPUTS}

Operating Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-14 on page 3-23.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

P_{INPUTS} = 0 W

I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$

Operating Mode

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-14 on page 3-23.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 3-15 on page 3-23.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$P_{OUTPUTS}$ = 0 W

RAM Dynamic Contribution—P_{MEMORY}

Operating Mode

$P_{MEMORY} = (N_{BLOCKS} * P_{AC11} * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * P_{AC12} * \beta_3 * F_{WRITE\text{-}CLOCK})$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 3-15 on page 3-23.

β_3 the RAM enable rate for write operations—guidelines are provided in Table 3-15 on page 3-23.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

Standby Mode and Sleep Mode

$P_{MEMORY} = 0$ W

PLL/CCC Dynamic Contribution—P_{PLL}

Operating Mode

$P_{PLL} = P_{AC13} * F_{CLKOUT}$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Standby Mode and Sleep Mode

$P_{PLL} = 0$ W

Nonvolatile Memory Dynamic Contribution—P_{NVM}

Operating Mode

The NVM dynamic power consumption is a piecewise linear function of frequency.

$P_{NVM} = N_{NVM\text{-}BLOCKS} * \beta_4 * P_{AC15} * F_{READ\text{-}NVM}$ when $F_{READ\text{-}NVM} \leq 33$ MHz,

$P_{NVM} = N_{NVM\text{-}BLOCKS} * \beta_4 *(P_{AC16} + P_{AC17} * F_{READ\text{-}NVM}$ when $F_{READ\text{-}NVM} > 33$ MHz

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks used in the design (2 inAFS600).

β_4 is the NVM enable rate for read operations. Default is 0 (NVM mainly in idle state).

$F_{READ\text{-}NVM}$ is the NVM read clock frequency.

Standby Mode and Sleep Mode

$P_{NVM} = 0$ W

Crystal Oscillator Dynamic Contribution—$P_{XTL\text{-}OSC}$

Operating Mode

$P_{XTL\text{-}OSC} = P_{AC18}$

Standby Mode

$P_{XTL\text{-}OSC} = P_{AC18}$

Sleep Mode

$P_{XTL\text{-}OSC} = 0$ W

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

RC Oscillator Dynamic Contribution—$P_{RC\text{-}OSC}$

Operating Mode

$P_{RC\text{-}OSC} = P_{AC19}$

Standby Mode and Sleep Mode

$P_{RC\text{-}OSC} = 0$ W

Analog System Dynamic Contribution—P_{AB}

Operating Mode

$P_{AB} = P_{AC20}$

Standby Mode and Sleep Mode

$P_{AB} = 0$ W

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

***Table 3-14* • Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

***Table 3-15* • Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%
β_4	NVM enable rate for read operations	0%

Example of Power Calculation

This example considers a shift register with 5,000 storage tiles, including a counter and memory that stores analog information. The shift register is clocked at 50 MHz and stores and reads information from a RAM.

The device used is a commercial AFS600 device operating in typical conditions.

The calculation below uses the power calculation methodology previously presented and shows how to determine the dynamic and static power consumption of resources used in the application.

Also included in the example is the calculation of power consumption in operating, standby, and sleep modes to illustrate the benefit of power-saving modes.

Global Clock Contribution—P_{CLOCK}

F_{CLK} = 50 MHz

Number of sequential VersaTiles: $N_{S\text{-}CELL}$ = 5,000

Estimated number of Spines: N_{SPINES} = 5

Estimated number of Rows: N_{ROW} = 313

Operating Mode

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * PAC3 + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

$P_{CLOCK} = (0.0128 + 5 * 0.0019 + 313 * 0.00081 + 5{,}000 * 0.00011) * 50$

P_{CLOCK} = 41.28 mW

Standby Mode and Sleep Mode

P_{CLOCK} = 0 W

Logic—Sequential Cells, Combinational Cells, and Routing Net Contributions—$P_{S\text{-}CELL}$, $P_{C\text{-}CELL}$, and P_{NET}

F_{CLK} = 50 MHz

Number of sequential VersaTiles: $N_{S\text{-}CELL}$ = 5,000

Number of combinatorial VersaTiles: $N_{C\text{-}CELL}$ = 6,000

Estimated toggle rate of VersaTile outputs: α_1 = 0.1 (10%)

Operating Mode

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + (\alpha_1 / 2) * P_{AC6}) * F_{CLK}$

$P_{S\text{-}CELL} = 5{,}000 * (0.00007 + (0.1 / 2) * 0.00029) * 50$

$P_{S\text{-}CELL}$ = 21.13 mW

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * P_{AC7} * F_{CLK}$

$P_{C\text{-}CELL} = 6{,}000 * (0.1 / 2) * 0.00029 * 50$

$P_{C\text{-}CELL}$ = 4.35 mW

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * P_{AC8} * F_{CLK}$

$P_{NET} = (5{,}000 + 6{,}000) * (0.1 / 2) * 0.0007 * 50$

P_{NET} = 19.25 mW

$P_{LOGIC} = P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET}$

P_{LOGIC} = 21.13 mW + 4.35 mW + 19.25 mW

P_{LOGIC} = 44.73 mW

Standby Mode and Sleep Mode

$P_{S\text{-}CELL}$ = 0 W

$P_{C\text{-}CELL}$ = 0 W

P_{NET} = 0 W

P_{LOGIC} = 0 W

I/O Input and Output Buffer Contribution—$P_{I/O}$

This example uses LVTTL 3.3 V I/O cells. The output buffers are 12 mA–capable, configured with high output slew and driving a 35 pF output load.

F_{CLK} = 50 MHz

Number of input pins used: N_{INPUTS} = 30

Number of output pins used: $N_{OUTPUTS}$ = 40

Estimated I/O buffer toggle rate: α_2 = 0.1 (10%)

Estimated IO buffer enable rate: β_1 = 1 (100%)

Operating Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * P_{AC9} * F_{CLK}$

$P_{INPUTS} = 30 * (0.1 / 2) * 0.01739 * 50$

P_{INPUTS} = 1.30 mW

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * P_{AC10} * F_{CLK}$

$P_{OUTPUTS} = 40 * (0.1 / 2) * 1 * 0.4747 * 50$

$P_{OUTPUTS}$ = 47.47 mW

$P_{I/O} = P_{INPUTS} + P_{OUTPUTS}$

$P_{I/O}$ = 1.30 mW + 47.47 mW

$P_{I/O}$ = 48.77 mW

Standby Mode and Sleep Mode

P_{INPUTS} = 0 W

$P_{OUTPUTS}$ = 0 W

$P_{I/O}$ = 0 W

RAM Contribution—P_{MEMORY}

Frequency of Read Clock: $F_{READ\text{-}CLOCK}$ = 10 MHz

Frequency of Write Clock: $F_{WRITE\text{-}CLOCK}$ = 10 MHz

Number of RAM blocks: N_{BLOCKS} = 20

Estimated RAM Read Enable Rate: β_2 = 0.125 (12.5%)

Estimated RAM Write Enable Rate: β_3 = 0.125 (12.5%)

Operating Mode

$P_{MEMORY} = (N_{BLOCKS} * P_{AC11} * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * P_{AC12} * \beta_3 * F_{WRITE\text{-}CLOCK})$

$P_{MEMORY} = (20 * 0.025 * 0.125 * 10) + (20 * 0.030 * 0.125 * 10)$

P_{MEMORY} = 1.38 mW

Standby Mode and Sleep Mode

P_{MEMORY} = 0 W

PLL/CCC Contribution—P_{PLL}

PLL is not used in this application.

P_{PLL} = 0 W

Nonvolatile Memory—P_{NVM}

Nonvolatile memory is not used in this application.

P_{NVM} = 0 W

Crystal Oscillator—$P_{XTL-OSC}$

The application utilizes standby mode. The crystal oscillator is assumed to be active.

Operating Mode

$P_{XTL-OSC} = P_{AC18}$

$P_{XTL-OSC}$ = 0.63 mW

Standby Mode

$P_{XTL-OSC} = P_{AC18}$

$P_{XTL-OSC}$ = 0.63 mW

Sleep Mode

$P_{XTL-OSC}$ = 0 W

RC Oscillator—P_{RC-OSC}

Operating Mode

$P_{RC-OSC} = P_{AC19}$

P_{RC-OSC} = 3.30 mW

Standby Mode and Sleep Mode

P_{RC-OSC} = 0 W

Analog System—P_{AB}

Number of Quads used: N_{QUADS} = 4

Operating Mode

$P_{AB} = P_{AC20}$

P_{AB} = 3.00 mW

Standby Mode and Sleep Mode

P_{AB} = 0 W

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL-OSC} + P_{RC-OSC} + P_{AB}$

P_{DYN} = 41.28 mW + 21.1 mW + 4.35 mW + 19.25 mW + 1.30 mW + 47.47 mW + 1.38 mW + 0 + 0 + 0.63 mW + 3.30 mW + 3.00 mW

P_{DYN} = 143.06 mW

Standby Mode

$P_{DYN} = P_{XTL-OSC}$

P_{DYN} = 0.63 mW

Sleep Mode

P_{DYN} = 0 W

Total Static Power Consumption—P_{STAT}

Number of Quads used: N_{QUADS} = 4

Number of NVM blocks available (AFS600): $N_{NVM-BLOCKS}$ = 2

Number of input pins used: N_{INPUTS} = 30

Number of output pins used: $N_{OUTPUTS}$ = 40

Operating Mode

$P_{STAT} = P_{DC1} + (N_{NVM-BLOCKS} * P_{DC4}) + P_{DC5} + (N_{QUADS} * P_{DC6}) + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8})$

P_{STAT} = 7.50 mW + (2 * 1.19 mW) + 8.25 mW + (4 * 3.30 mW) + (30 * 0.00) + (40 * 0.00)

P_{STAT} = 31.33 mW

Standby Mode

$P_{STAT} = P_{DC2}$

P_{STAT} = 0.03 mW

Sleep Mode

$P_{STAT} = P_{DC3}$

P_{STAT} = 0.03 mW

Total Power Consumption—P_{TOTAL}

In operating mode, the total power consumption of the device is 174.39 mW:

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{TOTAL} = 143.06 mW + 31.33 mW

P_{TOTAL} = 174.39 mW

In standby mode, the total power consumption of the device is limited to 0.66 mW:

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{TOTAL} = 0.03 mW + 0.63 mW

P_{TOTAL} = 0.66 mW

In sleep mode, the total power consumption of the device drops as low as 0.03 mW:

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{TOTAL} = 0.03 mW

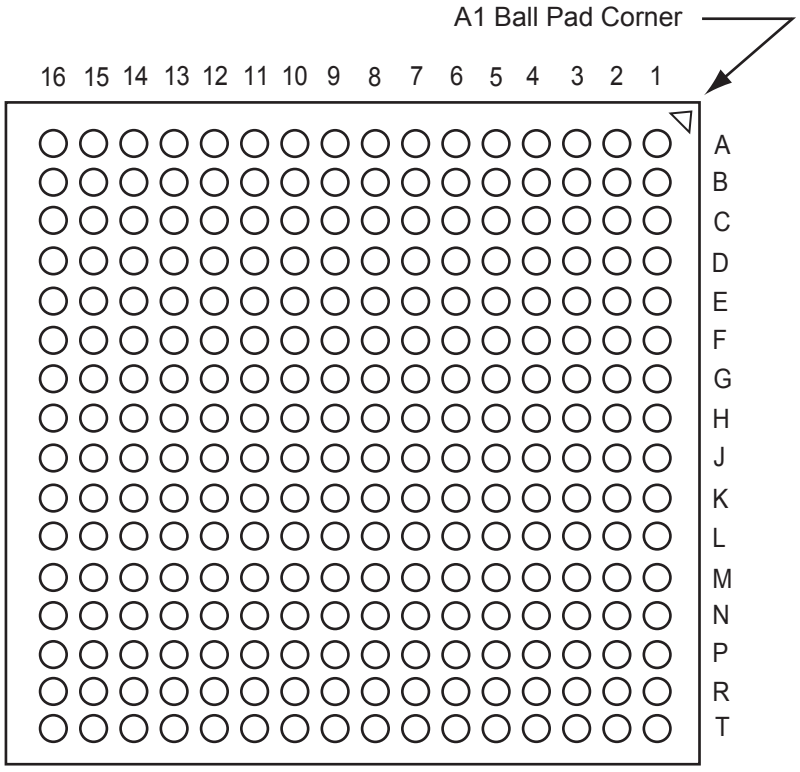
Power Consumption

Table 3-16 **• Power Consumption**

Parameter	Description	Condition	Min.	Typ	Max.	Units
Crystal Oscillator						
ISTBXTAL	Standby Current of Crystal Oscillator			10		µA
IDYNXTAL	Operating Current	RC		0.6		mA
		0.032–0.2		0.6		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
RC Oscillator						
IDYNRC	Operating Current			1		mA
ACM						
	Operating Current (fixed clock)			200		µA/MHz
	Operating Current (user clock)			30		µA
NVM System						
	NVM Array Operating Power	Idle		795		µA
		Read operation		See Table 3-11 on page 3-17.		See Table 3-11 on page 3-17.
		Erase		900		µA
		Write		900		µA
PNVMCTRL	NVM Controller Operating Power			20		µW/MHz

4 – Pin Assignments

256-Pin FBGA



Note

For Package Manufacturing and Environmental information, visit the Resource Center at www.actel.com/products/solutions/package/default.aspx.

256-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
A1	GND	GND
A2	VCCIB0	VCCIB0
A3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
A4	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0
A5	GND	GND
A6	IO10PDB0V1	IO07PDB0V1
A7	IO12PDB0V1	IO13PDB0V2
A8	IO12NDB0V1	IO13NDB0V2
A9	IO22NDB1V0	IO24NDB1V0
A10	IO22PDB1V0	IO24PDB1V0
A11	IO24NDB1V1	IO29NDB1V1
A12	GND	GND
A13	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2
A14	IO29NDB1V1	IO43NDB1V2
A15	VCCIB1	VCCIB1
A16	GND	GND
B1	V_{COMPLA}	VCOMPLA
B2	VCCPLA	VCCPLA
B3	IO00NDB0V0	IO00NDB0V0
B4	IO00PDB0V0	IO00PDB0V0
B5	GAB1/IO02PPB0V0	GAB1/IO02PPB0V0
B6	IO10NDB0V1	IO07NDB0V1
B7	VCCIB0	VCCIB0
B8	IO18NDB1V0	IO22NDB1V0
B9	IO18PDB1V0	IO22PDB1V0
B10	VCCIB1	VCCIB1
B11	IO24PDB1V1	IO29PDB1V1
B12	GBC0/IO26NPB1V1	GBC0/IO40NPB1V2
B13	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2
B14	IO29PDB1V1	IO43PDB1V2
B15	VCCPLB	VCCPLB
B16	VCOMPLB	VCOMPLB
C1	VCCIB4	VCCIB4
C2	GND	GND
C3	VCCIB4	VCCIB4
C4	VCCIB0	VCCIB0
C5	VCCIB0	VCCIB0

256-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
C6	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0
C7	IO06NDB0V0	IO09NDB0V1
C8	IO16PDB1V0	IO23PDB1V0
C9	IO16NDB1V0	IO23NDB1V0
C10	IO25NDB1V1	IO31NDB1V1
C11	IO25PDB1V1	IO31PDB1V1
C12	VCCIB1	VCCIB1
C13	GBC1/IO26PPB1V1	GBC1/IO40PPB1V2
C14	VCCIB2	VCCIB2
C15	GND	GND
C16	VCCIB2	VCCIB2
D1	IO84NDB4V0	IO124NDB4V0
D2	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0
D3	IO85NDB4V0	IO125NDB4V0
D4	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0
D5	GAB0/IO02NPB0V0	GAB0/IO02NPB0V0
D6	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0
D7	IO06PDB0V0	IO09PDB0V1
D8	IO14NDB0V1	IO15NDB0V2
D9	IO14PDB0V1	IO15PDB0V2
D10	IO23PDB1V1	IO37PDB1V2
D11	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2
D12	VCCIB1	VCCIB1
D13	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0
D14	IO30NDB2V0	IO44NDB2V0
D15	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0
D16	IO31NDB2V0	IO45NDB2V0
E1	GND	GND
E2	IO81NDB4V0	IO118NDB4V0
E3	IO81PDB4V0	IO118PDB4V0
E4	VCCIB4	VCCIB4
E5	IO83NPB4V0	IO123NPB4V0
E6	IO04NPB0V0	IO05NPB0V1
E7	GND	GND
E8	IO08PDB0V1	IO11PDB0V1
E9	IO20NDB1V0	IO27NDB1V1
E10	GND	GND

256-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
E11	GBB1/IO27PDB1V1	GBB1/IO41PDB1V2
E12	IO33PSB2V0	IO48PSB2V0
E13	VCCIB2	VCCIB2
E14	IO32NDB2V0	IO46NDB2V0
E15	GBC2/IO32PDB2V0	GBC2/IO46PDB2V0
E16	GND	GND
F1	IO79NDB4V0	IO111NDB4V0
F2	IO79PDB4V0	IO111PDB4V0
F3	IO76NDB4V0	IO112NDB4V0
F4	IO76PDB4V0	IO112PDB4V0
F5	IO82PSB4V0	IO120PSB4V0
F6	GAC2/IO83PPB4V0	GAC2/IO123PPB4V0
F7	IO04PPB0V0	IO05PPB0V1
F8	IO08NDB0V1	IO11NDB0V1
F9	IO20PDB1V0	IO27PDB1V1
F10	IO23NDB1V1	IO37NDB1V2
F11	IO36NDB2V0	IO50NDB2V0
F12	IO36PDB2V0	IO50PDB2V0
F13	IO39NDB2V0	IO59NDB2V0
F14	GCA2/IO39PDB2V0	GCA2/IO59PDB2V0
F15	GCB2/IO40PDB2V0	GCB2/IO60PDB2V0
F16	IO40NDB2V0	IO60NDB2V0
G1	IO74NPB4V0	IO109NPB4V0
G2	VCCIB4	VCCIB4
G3	GFB2/IO74PPB4V0	GFB2/IO109PPB4V0
G4	GFA2/IO75PDB4V0	GFA2/IO110PDB4V0
G5	GND	GND
G6	IO75NDB4V0	IO110NDB4V0
G7	GND	GND
G8	VCC	VCC
G9	GND	GND
G10	VCC	VCC
G11	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0
G12	GND	GND
G13	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0
G14	IO41NPB2V0	IO61NPB2V0
G15	VCCIB2	VCCIB2

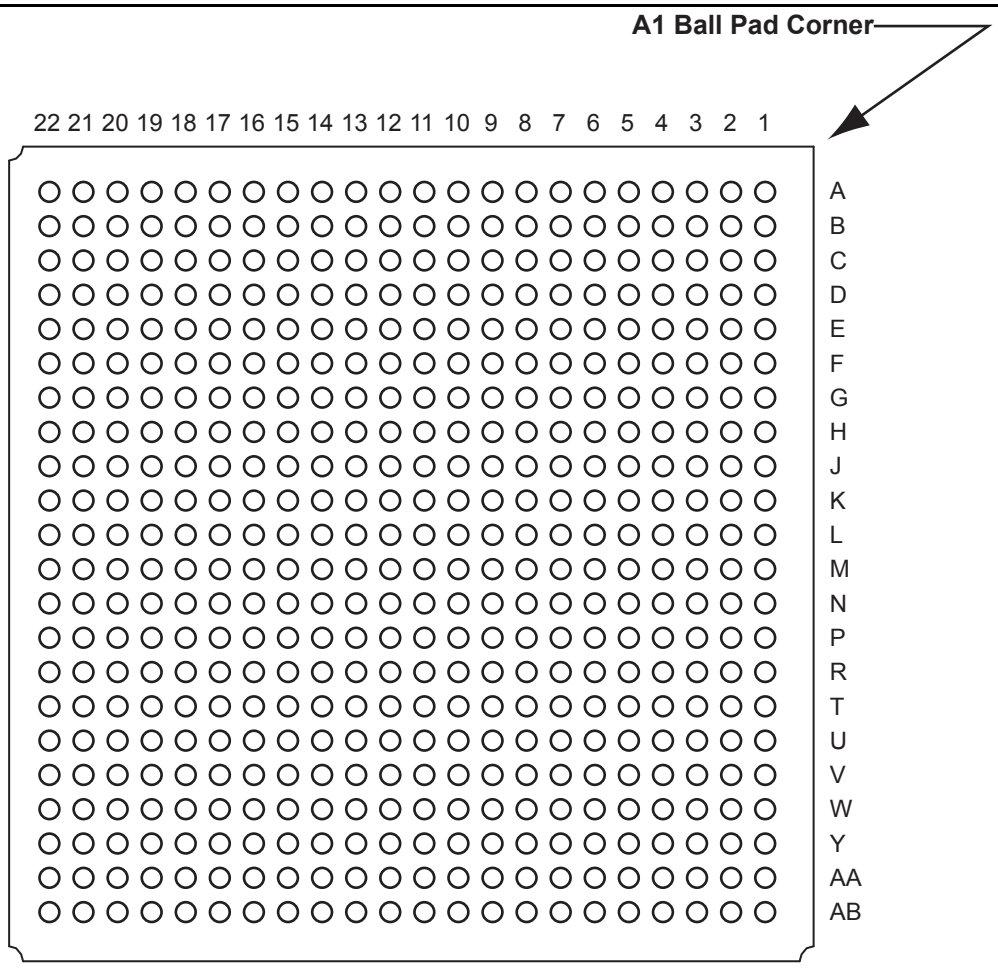
256-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
G16	GCC2/IO41PPB2V0	GCC2/IO61PPB2V0
H1	GFC2/IO73PDB4V0	GFC2/IO108PDB4V0
H2	IO73NDB4V0	IO108NDB4V0
H3	XTAL2	XTAL2
H4	XTAL1	XTAL1
H5	GNDOSC	GNDOSC
H6	VCCOSC	VCCOSC
H7	VCC	VCC
H8	GND	GND
H9	VCC	VCC
H10	GND	GND
H11	IO47NDB2V0	IO69NDB2V0
H12	IO47PDB2V0	IO69PDB2V0
H13	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0
H14	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0
H15	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0
H16	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0
J1	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0
J2	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0
J3	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0
J4	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0
J5	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0
J6	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0
J7	GND	GND
J8	VCC	VCC
J9	GND	GND
J10	VCC	VCC
J11	IO56NPB2V0	IO83NPB2V0
J12	GDB0/IO53NPB2V0	GDB0/IO80NPB2V0
J13	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0
J14	GDC1/IO52PPB2V0	GDC1/IO79PPB2V0
J15	IO51NSB2V0	IO77NSB2V0
J16	GDC0/IO52NPB2V0	GDC0/IO79NPB2V0
K1	IO67NPB4V0	IO92NPB4V0
K2	VCCIB4	VCCIB4
K3	IO67PPB4V0	IO92PPB4V0
K4	IO65PDB4V0	IO96PDB4V0

256-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
K5	GND	GND
K6	IO65NDB4V0	IO96NDB4V0
K7	VCC	VCC
K8	GND	GND
K9	VCC	VCC
K10	GND	GND
K11	GDC2/IO57PPB2V0	GDC2/IO84PPB2V0
K12	GND	GND
K13	GDA0/IO54NDB2V0	GDA0/IO81NDB2V0
K14	GDA2/IO55PPB2V0	GDA2/IO82PPB2V0
K15	VCCIB2	VCCIB2
K16	GDB1/IO53PPB2V0	GDB1/IO80PPB2V0
L1	GEC1/IO63PDB4V0	GEC1/IO90PDB4V0
L2	GEC0/IO63NDB4V0	GEC0/IO90NDB4V0
L3	GEB1/IO62PDB4V0	GEB1/IO89PDB4V0
L4	GEB0/IO62NDB4V0	GEB0/IO89NDB4V0
L5	IO60NDB4V0	IO87NDB4V0
L6	GEC2/IO60PDB4V0	GEC2/IO87PDB4V0
L7	GNDA	GNDA
L8	AC2	AC2
L9	AV4	AV4
L10	AC5	AC5
L11	PTEM	PTEM
L12	TDO	TDO
L13	VJTAG	VJTAG
L14	IO57NPB2V0	IO84NPB2V0
L15	GDB2/IO56PPB2V0	GDB2/IO83PPB2V0
L16	IO55NPB2V0	IO82NPB2V0
M1	GND	GND
M2	GEA1/IO61PDB4V0	GEA1/IO88PDB4V0
M3	GEA0/IO61NDB4V0	GEA0/IO88NDB4V0
M4	VCCIB4	VCCIB4
M5	IO58NPB4V0	IO85NPB4V0
M6	AV0	AV0
M7	AC1	AC1
M8	AG3	AG3
M9	AC4	AC4

256-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
M10	AC6	AC6
M11	AG7	AG7
M12	VPUMP	VPUMP
M13	VCCIB2	VCCIB2
M14	TMS	TMS
M15	TRST	TRST
M16	GND	GND
N1	GEB2/IO59PDB4V0	GEB2/IO86PDB4V0
N2	IO59NDB4V0	IO86NDB4V0
N3	GEA2/IO58PPB4V0	GEA2/IO85PPB4V0
N4	VCC33PMP	VCC33PMP
N5	VCC15A	VCC15A
N6	AG0	AG0
N7	AC3	AC3
N8	AG5	AG5
N9	AV5	AV5
N10	AG6	AG6
N11	AC8	AC8
N12	GNDA	GNDA
N13	VCC33A	VCC33A
N14	VCCNVM	VCCNVM
N15	TCK	TCK
N16	TDI	TDI
P1	VCCNVM	VCCNVM
P2	GNDNVM	GNDNVM
P3	GNDA	GNDA
P4	AC0	AC0
P5	AG1	AG1
P6	AV1	AV1
P7	AG2	AG2
P8	AG4	AG4
P9	GNDA	GNDA
P10	AC7	AC7
P11	AV8	AV8
P12	AG8	AG8
P13	AV9	AV9
P14	ADCGNDREF	ADCGNDREF

256-Pin FBGA		
Pin Number	**AFS600 Function**	**AFS1500 Function**
P15	PTBASE	PTBASE
P16	GNDNVM	GNDNVM
R1	VCCIB4	VCCIB4
R2	PCAP	PCAP
R3	AT1	AT1
R4	AT0	AT0
R5	AV2	AV2
R6	AT2	AT2
R7	AV3	AV3
R8	AT5	AT5
R9	AV6	AV6
R10	AT7	AT7
R11	AV7	AV7
R12	AT9	AT9
R13	AG9	AG9
R14	AC9	AC9
R15	PUB	PUB
R16	VCCIB2	VCCIB2
T1	GND	GND
T2	NCAP	NCAP
T3	VCC33N	VCC33N
T4	ATRTN0	ATRTN0
T5	AT3	AT3
T6	ATRTN1	ATRTN1
T7	AT4	AT4
T8	ATRTN2	ATRTN2
T9	AT6	AT6
T10	ATRTN3	ATRTN3
T11	AT8	AT8
T12	ATRTN4	ATRTN4
T13	GNDA	GNDA
T14	VCC33A	VCC33A
T15	VAREF	VAREF
T16	GND	GND

484-Pin FBGA



Note

For Package Manufacturing and Environmental information, visit the Resource Center at www.actel.com/products/solutions/package/default.aspx.

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
A1	GND	GND
A2	VCC	NC
A3	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0
A4	GAB0/IO02NDB0V0	GAB0/IO02NDB0V0
A5	GAB1/IO02PDB0V0	GAB1/IO02PDB0V0
A6	IO07NDB0V1	IO07NDB0V1
A7	IO07PDB0V1	IO07PDB0V1
A8	IO10PDB0V1	IO09PDB0V1
A9	IO14NDB0V1	IO13NDB0V2
A10	IO14PDB0V1	IO13PDB0V2
A11	IO17PDB1V0	IO24PDB1V0
A12	IO18PDB1V0	IO26PDB1V0
A13	IO19NDB1V0	IO27NDB1V1
A14	IO19PDB1V0	IO27PDB1V1
A15	IO24NDB1V1	IO35NDB1V2
A16	IO24PDB1V1	IO35PDB1V2
A17	GBC0/IO26NDB1V1	GBC0/IO40NDB1V2
A18	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2
A19	IO29NDB1V1	IO43NDB1V2
A20	IO29PDB1V1	IO43PDB1V2
A21	VCC	NC
A22	GND	GND
AA1	VCC	NC
AA2	GND	GND
AA3	VCCIB4	VCCIB4
AA4	VCCIB4	VCCIB4
AA5	PCAP	PCAP
AA6	AG0	AG0
AA7	GNDA	GNDA
AA8	AG1	AG1
AA9	AG2	AG2
AA10	GNDA	GNDA
AA11	AG3	AG3
AA12	AG6	AG6
AA13	GNDA	GNDA

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
AA14	AG7	AG7
AA15	AG8	AG8
AA16	GNDA	GNDA
AA17	AG9	AG9
AA18	VAREF	VAREF
AA19	VCCIB2	VCCIB2
AA20	PTEM	PTEM
AA21	GND	GND
AA22	VCC	NC
AB1	GND	GND
AB2	VCC	NC
AB3	NC	IO94NSB4V0
AB4	GND	GND
AB5	VCC33N	VCC33N
AB6	AT0	AT0
AB7	ATRTN0	ATRTN0
AB8	AT1	AT1
AB9	AT2	AT2
AB10	ATRTN1	ATRTN1
AB11	AT3	AT3
AB12	AT6	AT6
AB13	ATRTN3	ATRTN3
AB14	AT7	AT7
AB15	AT8	AT8
AB16	ATRTN4	ATRTN4
AB17	AT9	AT9
AB18	VCC33A	VCC33A
AB19	GND	GND
AB20	NC	IO76NPB2V0
AB21	VCC	NC
AB22	GND	GND
B1	VCC	NC
B2	GND	GND
B3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
B4	GND	GND

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
B5	IO05NDB0V0	IO04NDB0V0
B6	IO05PDB0V0	IO04PDB0V0
B7	GND	GND
B8	IO10NDB0V1	IO09NDB0V1
B9	IO13PDB0V1	IO11PDB0V1
B10	GND	GND
B11	IO17NDB1V0	IO24NDB1V0
B12	IO18NDB1V0	IO26NDB1V0
B13	GND	GND
B14	IO21NDB1V0	IO31NDB1V1
B15	IO21PDB1V0	IO31PDB1V1
B16	GND	GND
B17	GBC1/IO26PDB1V1	GBC1/IO40PDB1V2
B18	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2
B19	GND	GND
B20	VCCPLB	VCCPLB
B21	GND	GND
B22	VCC	NC
C1	IO82PDB4V0	IO121PDB4V0
C2	NC	IO122PSB4V0
C3	IO00NDB0V0	IO00NDB0V0
C4	IO00PDB0V0	IO00PDB0V0
C5	VCCIB0	VCCIB0
C6	IO06NDB0V0	IO05NDB0V1
C7	IO06PDB0V0	IO05PDB0V1
C8	VCCIB0	VCCIB0
C9	IO13NDB0V1	IO11NDB0V1
C10	IO11PDB0V1	IO14PDB0V2
C11	VCCIB0	VCCIB0
C12	VCCIB1	VCCIB1
C13	IO20NDB1V0	IO29NDB1V1
C14	IO20PDB1V0	IO29PDB1V1
C15	VCCIB1	VCCIB1
C16	IO25NDB1V1	IO37NDB1V2
C17	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
C18	VCCIB1	VCCIB1
C19	VCOMPLB	VCOMPLB
C20	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0
C21	NC	IO48PSB2V0
C22	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0
D1	IO82NDB4V0	IO121NDB4V0
D2	GND	GND
D3	IO83NDB4V0	IO123NDB4V0
D4	GAC2/IO83PDB4V0	GAC2/IO123PDB4V0
D5	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0
D6	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0
D7	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0
D8	IO09NDB0V1	IO10NDB0V1
D9	IO09PDB0V1	IO10PDB0V1
D10	IO11NDB0V1	IO14NDB0V2
D11	IO16NDB1V0	IO23NDB1V0
D12	IO16PDB1V0	IO23PDB1V0
D13	NC	IO32NPB1V1
D14	IO23NDB1V1	IO34NDB1V1
D15	IO23PDB1V1	IO34PDB1V1
D16	IO25PDB1V1	IO37PDB1V2
D17	GBB1/IO27PDB1V1	GBB1/IO41PDB1V2
D18	VCCIB2	VCCIB2
D19	NC	IO47PPB2V0
D20	IO30NDB2V0	IO44NDB2V0
D21	GND	GND
D22	IO31NDB2V0	IO45NDB2V0
E1	IO81NDB4V0	IO120NDB4V0
E2	IO81PDB4V0	IO120PDB4V0
E3	VCCIB4	VCCIB4
E4	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0
E5	IO85NDB4V0	IO125NDB4V0
E6	GND	GND
E7	VCCIB0	VCCIB0
E8	NC	IO08NDB0V1

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
E9	NC	IO08PDB0V1
E10	GND	GND
E11	IO15NDB1V0	IO22NDB1V0
E12	IO15PDB1V0	IO22PDB1V0
E13	GND	GND
E14	NC	IO32PPB1V1
E15	NC	IO36NPB1V2
E16	VCCIB1	VCCIB1
E17	GND	GND
E18	NC	IO47NPB2V0
E19	IO33PDB2V0	IO49PDB2V0
E20	VCCIB2	VCCIB2
E21	IO32NDB2V0	IO46NDB2V0
E22	GBC2/IO32PDB2V0	GBC2/IO46PDB2V0
F1	IO80NDB4V0	IO118NDB4V0
F2	IO80PDB4V0	IO118PDB4V0
F3	NC	IO119NSB4V0
F4	IO84NDB4V0	IO124NDB4V0
F5	GND	GND
F6	VCOMPLA	VCOMPLA
F7	VCCPLA	VCCPLA
F8	VCCIB0	VCCIB0
F9	IO08NDB0V1	IO12NDB0V1
F10	IO08PDB0V1	IO12PDB0V1
F11	VCCIB0	VCCIB0
F12	VCCIB1	VCCIB1
F13	IO22NDB1V0	IO30NDB1V1
F14	IO22PDB1V0	IO30PDB1V1
F15	VCCIB1	VCCIB1
F16	NC	IO36PPB1V2
F17	NC	IO38NPB1V2
F18	GND	GND
F19	IO33NDB2V0	IO49NDB2V0
F20	IO34PDB2V0	IO50PDB2V0
F21	IO34NDB2V0	IO50NDB2V0

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
F22	IO35PDB2V0	IO51PDB2V0
G1	IO77PDB4V0	IO115PDB4V0
G2	GND	GND
G3	IO78NDB4V0	IO116NDB4V0
G4	IO78PDB4V0	IO116PDB4V0
G5	VCCIB4	VCCIB4
G6	NC	IO117PDB4V0
G7	VCCIB4	VCCIB4
G8	GND	GND
G9	IO04NDB0V0	IO06NDB0V1
G10	IO04PDB0V0	IO06PDB0V1
G11	IO12NDB0V1	IO16NDB0V2
G12	IO12PDB0V1	IO16PDB0V2
G13	NC	IO28NDB1V1
G14	NC	IO28PDB1V1
G15	GND	GND
G16	NC	IO38PPB1V2
G17	NC	IO53PDB2V0
G18	VCCIB2	VCCIB2
G19	IO36PDB2V0	IO52PDB2V0
G20	IO36NDB2V0	IO52NDB2V0
G21	GND	GND
G22	IO35NDB2V0	IO51NDB2V0
H1	IO77NDB4V0	IO115NDB4V0
H2	IO76PDB4V0	IO113PDB4V0
H3	VCCIB4	VCCIB4
H4	IO79NDB4V0	IO114NDB4V0
H5	IO79PDB4V0	IO114PDB4V0
H6	NC	IO117NDB4V0
H7	GND	GND
H8	VCC	VCC
H9	VCCIB0	VCCIB0
H10	GND	GND
H11	VCCIB0	VCCIB0
H12	VCCIB1	VCCIB1

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
H13	GND	GND
H14	VCCIB1	VCCIB1
H15	GND	GND
H16	GND	GND
H17	NC	IO53NDB2V0
H18	IO38PDB2V0	IO57PDB2V0
H19	GCA2/IO39PDB2V0	GCA2/IO59PDB2V0
H20	VCCIB2	VCCIB2
H21	IO37NDB2V0	IO54NDB2V0
H22	IO37PDB2V0	IO54PDB2V0
J1	NC	IO112PPB4V0
J2	IO76NDB4V0	IO113NDB4V0
J3	GFB2/IO74PDB4V0	GFB2/IO109PDB4V0
J4	GFA2/IO75PDB4V0	GFA2/IO110PDB4V0
J5	NC	IO112NPB4V0
J6	NC	IO104PDB4V0
J7	NC	IO111PDB4V0
J8	VCCIB4	VCCIB4
J9	GND	GND
J10	VCC	VCC
J11	GND	GND
J12	VCC	VCC
J13	GND	GND
J14	VCC	VCC
J15	VCCIB2	VCCIB2
J16	GCB2/IO40PDB2V0	GCB2/IO60PDB2V0
J17	NC	IO58NDB2V0
J18	IO38NDB2V0	IO57NDB2V0
J19	IO39NDB2V0	IO59NDB2V0
J20	GCC2/IO41PDB2V0	GCC2/IO61PDB2V0
J21	NC	IO55PSB2V0
J22	IO42PDB2V0	IO56PDB2V0
K1	GFC2/IO73PDB4V0	GFC2/IO108PDB4V0
K2	GND	GND
K3	IO74NDB4V0	IO109NDB4V0

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
K4	IO75NDB4V0	IO110NDB4V0
K5	GND	GND
K6	NC	IO104NDB4V0
K7	NC	IO111NDB4V0
K8	GND	GND
K9	VCC	VCC
K10	GND	GND
K11	VCC	VCC
K12	GND	GND
K13	VCC	VCC
K14	GND	GND
K15	GND	GND
K16	IO40NDB2V0	IO60NDB2V0
K17	NC	IO58PDB2V0
K18	GND	GND
K19	NC	IO68NPB2V0
K20	IO41NDB2V0	IO61NDB2V0
K21	GND	GND
K22	IO42NDB2V0	IO56NDB2V0
L1	IO73NDB4V0	IO108NDB4V0
L2	VCCOSC	VCCOSC
L3	VCCIB4	VCCIB4
L4	XTAL2	XTAL2
L5	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0
L6	VCCIB4	VCCIB4
L7	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0
L8	VCCIB4	VCCIB4
L9	GND	GND
L10	VCC	VCC
L11	GND	GND
L12	VCC	VCC
L13	GND	GND
L14	VCC	VCC
L15	VCCIB2	VCCIB2
L16	IO48PDB2V0	IO70PDB2V0

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
L17	VCCIB2	VCCIB2
L18	IO46PDB2V0	IO69PDB2V0
L19	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0
L20	VCCIB2	VCCIB2
L21	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0
L22	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0
M1	NC	IO103PDB4V0
M2	XTAL1	XTAL1
M3	VCCIB4	VCCIB4
M4	GNDOSC	GNDOSC
M5	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0
M6	VCCIB4	VCCIB4
M7	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0
M8	VCCIB4	VCCIB4
M9	VCC	VCC
M10	GND	GND
M11	VCC	VCC
M12	GND	GND
M13	VCC	VCC
M14	GND	GND
M15	VCCIB2	VCCIB2
M16	IO48NDB2V0	IO70NDB2V0
M17	VCCIB2	VCCIB2
M18	IO46NDB2V0	IO69NDB2V0
M19	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0
M20	VCCIB2	VCCIB2
M21	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0
M22	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0
N1	NC	IO103NDB4V0
N2	GND	GND
N3	IO68PDB4V0	IO101PDB4V0
N4	NC	IO100NPB4V0
N5	GND	GND
N6	NC	IO99PDB4V0
N7	NC	IO97PDB4V0

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
N8	GND	GND
N9	GND	GND
N10	VCC	VCC
N11	GND	GND
N12	VCC	VCC
N13	GND	GND
N14	VCC	VCC
N15	GND	GND
N16	GDB2/IO56PDB2V0	GDB2/IO83PDB2V0
N17	NC	IO78PDB2V0
N18	GND	GND
N19	IO47NDB2V0	IO72NDB2V0
N20	IO47PDB2V0	IO72PDB2V0
N21	GND	GND
N22	IO49PDB2V0	IO71PDB2V0
P1	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0
P2	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0
P3	IO68NDB4V0	IO101NDB4V0
P4	IO65PDB4V0	IO96PDB4V0
P5	IO65NDB4V0	IO96NDB4V0
P6	NC	IO99NDB4V0
P7	NC	IO97NDB4V0
P8	VCCIB4	VCCIB4
P9	VCC	VCC
P10	GND	GND
P11	VCC	VCC
P12	GND	GND
P13	VCC	VCC
P14	GND	GND
P15	VCCIB2	VCCIB2
P16	IO56NDB2V0	IO83NDB2V0
P17	NC	IO78NDB2V0
P18	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0
P19	GDB1/IO53PDB2V0	GDB1/IO80PDB2V0
P20	IO51NDB2V0	IO73NDB2V0

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
P21	IO51PDB2V0	IO73PDB2V0
P22	IO49NDB2V0	IO71NDB2V0
R1	IO69PDB4V0	IO102PDB4V0
R2	IO69NDB4V0	IO102NDB4V0
R3	VCCIB4	VCCIB4
R4	IO64PDB4V0	IO91PDB4V0
R5	IO64NDB4V0	IO91NDB4V0
R6	NC	IO92PDB4V0
R7	GND	GND
R8	GND	GND
R9	VCC33A	VCC33A
R10	GNDA	GNDA
R11	VCC33A	VCC33A
R12	GNDA	GNDA
R13	VCC33A	VCC33A
R14	GNDA	GNDA
R15	VCC	VCC
R16	GND	GND
R17	NC	IO74NDB2V0
R18	GDA0/IO54NDB2V0	GDA0/IO81NDB2V0
R19	GDB0/IO53NDB2V0	GDB0/IO80NDB2V0
R20	VCCIB2	VCCIB2
R21	IO50NDB2V0	IO75NDB2V0
R22	IO50PDB2V0	IO75PDB2V0
T1	NC	IO100PPB4V0
T2	GND	GND
T3	IO66PDB4V0	IO95PDB4V0
T4	IO66NDB4V0	IO95NDB4V0
T5	VCCIB4	VCCIB4
T6	NC	IO92NDB4V0
T7	GNDNVM	GNDNVM
T8	GNDA	GNDA
T9	NC	NC
T10	AV4	AV4
T11	NC	NC

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
T12	AV5	AV5
T13	AC5	AC5
T14	NC	NC
T15	GNDA	GNDA
T16	NC	IO77PPB2V0
T17	NC	IO74PDB2V0
T18	VCCIB2	VCCIB2
T19	IO55NDB2V0	IO82NDB2V0
T20	GDA2/IO55PDB2V0	GDA2/IO82PDB2V0
T21	GND	GND
T22	GDC1/IO52PDB2V0	GDC1/IO79PDB2V0
U1	IO67PDB4V0	IO98PDB4V0
U2	IO67NDB4V0	IO98NDB4V0
U3	GEC1/IO63PDB4V0	GEC1/IO90PDB4V0
U4	GEC0/IO63NDB4V0	GEC0/IO90NDB4V0
U5	GND	GND
U6	VCCNVM	VCCNVM
U7	VCCIB4	VCCIB4
U8	VCC15A	VCC15A
U9	GNDA	GNDA
U10	AC4	AC4
U11	VCC33A	VCC33A
U12	GNDA	GNDA
U13	AG5	AG5
U14	GNDA	GNDA
U15	PUB	PUB
U16	VCCIB2	VCCIB2
U17	TDI	TDI
U18	GND	GND
U19	IO57NDB2V0	IO84NDB2V0
U20	GDC2/IO57PDB2V0	GDC2/IO84PDB2V0
U21	NC	IO77NPB2V0
U22	GDC0/IO52NDB2V0	GDC0/IO79NDB2V0
V1	GEB1/IO62PDB4V0	GEB1/IO89PDB4V0
V2	GEB0/IO62NDB4V0	GEB0/IO89NDB4V0

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
V3	VCCIB4	VCCIB4
V4	GEA1/IO61PDB4V0	GEA1/IO88PDB4V0
V5	GEA0/IO61NDB4V0	GEA0/IO88NDB4V0
V6	GND	GND
V7	VCC33PMP	VCC33PMP
V8	NC	NC
V9	VCC33A	VCC33A
V10	AG4	AG4
V11	AT4	AT4
V12	ATRTN2	ATRTN2
V13	AT5	AT5
V14	VCC33A	VCC33A
V15	NC	NC
V16	VCC33A	VCC33A
V17	GND	GND
V18	TMS	TMS
V19	VJTAG	VJTAG
V20	VCCIB2	VCCIB2
V21	TRST	TRST
V22	TDO	TDO
W1	NC	IO93PDB4V0
W2	GND	GND
W3	NC	IO93NDB4V0
W4	GEB2/IO59PDB4V0	GEB2/IO86PDB4V0
W5	IO59NDB4V0	IO86NDB4V0
W6	AV0	AV0
W7	GNDA	GNDA
W8	AV1	AV1
W9	AV2	AV2
W10	GNDA	GNDA
W11	AV3	AV3
W12	AV6	AV6
W13	GNDA	GNDA
W14	AV7	AV7
W15	AV8	AV8

484-Pin FBGA		
Pin Number	AFS600 Function	AFS1500 Function
W16	GNDA	GNDA
W17	AV9	AV9
W18	VCCIB2	VCCIB2
W19	NC	IO68PPB2V0
W20	TCK	TCK
W21	GND	GND
W22	NC	IO76PPB2V0
Y1	GEC2/IO60PDB4V0	GEC2/IO87PDB4V0
Y2	IO60NDB4V0	IO87NDB4V0
Y3	GEA2/IO58PDB4V0	GEA2/IO85PDB4V0
Y4	IO58NDB4V0	IO85NDB4V0
Y5	NCAP	NCAP
Y6	AC0	AC0
Y7	VCC33A	VCC33A
Y8	AC1	AC1
Y9	AC2	AC2
Y10	VCC33A	VCC33A
Y11	AC3	AC3
Y12	AC6	AC6
Y13	VCC33A	VCC33A
Y14	AC7	AC7
Y15	AC8	AC8
Y16	VCC33A	VCC33A
Y17	AC9	AC9
Y18	ADCGNDREF	ADCGNDREF
Y19	PTBASE	PTBASE
Y20	GNDNVM	GNDNVM
Y21	VCCNVM	VCCNVM
Y22	VPUMP	VPUMP

5 – Datasheet Information

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "Fusion Device Status" table on page III, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows::

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

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